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# Design of resolution/power controllable Asynchronous Sigma-Delta Modulator

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**Abstract**

This paper presents the design of a Programmable Asynchronous Modulator (PAM) with field control of resolution and power. A novel variable hysteresis Schmitt Trigger (ST) is used for external programmability. Asynchronous Sigma-Delta Modulator (ASDM) implementation with external control voltages is proposed to supervise the resolution and power. This architecture with reduced circuit complexity considerably improves the earlier realizations by eliminating multiple current sources as well switched capacitor circuits and results in power saving up to 87 %. Proposed PAM design demonstrates an improved SNDR of 115 dB, DR of 96 dB, and power consumption below 280 μW. It illustrates Effective Number of Bits (ENOB) to 18.81 and Figure of Merit (FoM) to 0.15 fJ/conversion step. Modulator is implemented in Cadence UMC Hspice 0.18 μm CMOS analog technology. Off-chip PAM control for resolution/power performance has potential applications in battery operated ultra low power applications like IoT; where ADC is one of the major power consuming components. It offers the promise for an efficient performance with power saving.

**Keywords:** Asynchronous circuit, Sigma-Delta Modulator, Schmitt-Trigger, Tunable hysteresis, CMOS analog technology

## 1 Introduction

With CMOS technology scaling, circuit implementation faces various challenges in integrating analog and mixed signal circuits. Reduced dimensions with low power, impacts negatively on analog and mixed-signal circuit performances. Particularly; transistors at non-optimal operating points, leak the currents through transistor gates. It leads to reduced input voltage swings and nonlinearity; during analog signal processing. Additional implementation challenges are imposed when analog and mixed signal processing functions must coexist with digital circuits. The switching noise from digital circuitry may couple into the analog blocks; thus corrupting the analog information [1].

With nano-scale technology, the major thrust is on design with reduced analog circuits; making Sigma-Delta Modulator (SDM) as one of the most popular architectures for ADC. SDM implementation is less sensitive to analog circuit imperfections due to reduced design complexity, oversampling and noise shaping techniques [2]. This inexpensive system also meets the constraints like compact design, minimum power, less noise and reduced conversion time. SDM performance can be further improved for power reduction by using asynchronous sampling technique.

ADCs using synchronous modulators, sample the input with minimum Nyquist rate decided by the maximum signal variation. As a result, most of the power is wasted; in signal processing terms, the signal is non-stationary and therefore the optimal sampling rate should be adapted based on the signal characteristics [3]. As many real-world signals vary irregularly, and asynchronous circuit processes only these relevant brief periods. It reduces the circuit activity and thus the dynamic power consumption. Also, the asynchronous modulator implementation is clockless and eliminates clock jitter as well the high-frequency injection problems. Since the restrictions imposed by a regular clock are not present in Asynchronous Sigma-Delta Modulator (ASDM), the requirements on the settling (bandwidth) and slew rate of the op-amps are significantly reduced [4]. Compared to synchronous modulators, it has other advantages like low susceptibility to Electro Magnetic Interferences (EMI), immunity to metastability, low power dissipation and recursive signal reconstruction etc. [5–7]. Thus, ASDM proved to be an efficient implementation.

ASDM dynamic power consumption depends on the resolution, alternatively on the switching activity. Minimum switching activity leads to minimum power consumption. So, to program the ASDM for minimum switching activity,

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hysteresis modulation with external control is implemented in the proposed design. This approach improves Signal-to-Noise Ratio (SNR) and Dynamic Range (DR) with reduced power and area over reported implementations [8, 9]. Here, we present the complete design implementation of a resolution/power controllable and performance efficient Programmable Asynchronous Modulator (PAM). IoT devices like tiny sensors in thermostats, smoke detectors, entries to a house, sensors on the bridges, moisture sensors in a farm, mobile health monitors, or even cellphones are almost all battery-operated devices and spend most of their time in sleep or off condition. Connectivity in IoT is a new way of doing things, hence need to enable additional modes of operation specifically deep-sleep modes need to enable very fast shut down and wake-up time. So, PAM can preferably be used over sleep mode circuits having faster wake-up times. With proposed modulator, the external control over the ADC performance can be effectively used in ultra low power analog interfaces getting popular with IoT.

The rest of the paper is structured as follows. Background in Section 2 gives the development with short summary of reported ASDM literature. Section 3 presents the Proposed Work. Section 4 explains the enhanced ASDM architecture for the proposed PAM implementation. Section 5 provides the Principle of PAM operation. The block level implementation of PAM with analysis is presented in Section 6. Device level implementation with analysis is discussed in Section 7. Results with power/performance efficiency are presented in Section 8. The paper is concluded in Section 9.

## 2 Background

Asynchronous Sigma-Delta ADC (ASD-ADC) development is still an emergent research area. Dariusz Kos´cielnik and Marek Mis´kowicz presented, ASD-ADC implementation based on charge pump integrator which uses the current sources with varying efficiency. The presented model is not optimal either in terms of the modulator performance, the energy consumption, or possible circuit integration [7]. The MATLAB model of ASD-ADC consisting of ASDM followed by TDC is presented with simulation results by Tomislav Matic, Tomislav Svedek and Davor Vinko in [10]. ASDM analysis using precision timer by Mohammadmehdi Kafashan, Sajjad Beygi, and Farrokh Marvasti proved that SNR depends on iteration number and timer precision [11]. Kazuki Kuribayashi, Kazuya Machida, and Yuji Toyama proposed the device level implementation of ASDM by using current-mode circuits to obtain a large dynamic range, while keeping the node voltage variation as small as possible [12]. Overall ASDM is still in a developing stage.

To achieve the significant improvement in performance, merely few ASDM designs have been reported. In context to the reduction of ADC activity and energy consumption, we have already proposed the low-power ASDM implementation with hysteresis control [9]. It presents power-frequency-hysteresis analysis. It has achieved noticeable power-saving due to reduced power supply and bias currents. To modify the hysteresis, Schmitt Trigger (ST) uses various current sources with two switches. Implementation achieved maximum SNR of 60 dB at 2 MHz with hysteresis of 0.02 V. Limited SNR was attributable to nonidealities like: limited slew rate due to integrator nonlinearity, limited dc gain, and thermal noise due to switching activity. Also, the use of multiple current sources with switches did not provide energy/area efficient implementation in [9].

Considering these aspects, further, we proposed an improved ASDM design by implementing the self-timed quantizer for audio signals [13]. This ASDM scheme uses novel ST with externally tunable hysteresis. It allows the control on regenerative feedback current and thus on hysteresis level. Depending on input signal speed, we can externally set the resolution without corrupting inband spectrum. Thus, it enables the control on dynamic power consumption. This paper analyses SNDR variation with control voltage and selection of optimized Over Cycling Ratio (OCR). Current work extends the design of [13] for frequency range up to 2 MHz and comprehensively presents the performance analyses. The major problem of using multiple current sources with switches is solved in the proposed design by using externally variable control voltages.

## 3 Proposed Work

Here, we propose the complete design of a Programmable Asynchronous Modulator (PAM) implementation on system and device level; with power/performance analysis. Design is based on asynchronous sigma-delta concept but with a use of novel Current Regenerative Schmitt Trigger (CRST). With irregular signals, depending on signal slope or frequency; hysteresis can be programmed just by adjusting the external control voltages. This is to gain the control over regenerative feedback current and hence the step size. Consequently, the resolution can be set to reduce the dynamic power consumption. Proposed design makes it possible to program the ASDM even after fabrication. It simply modulates hysteresis to improve the frequency range and provide external control on dynamic power. The graphical analysis for Signal-to-Noise and Distortion Ratio (SNDR), Dynamic Range (DR), and average power consumption with hysteresis modulation is comprehensively presented. Performance is compared to the reported literatures. The proposed improved design is simple yet effective with a new concept implemented for ASDM. Essentially, we enhanced the ASDM architecture for the proposed PAM design.

## 4 Enhanced ASDM architecture

Modulator converts an analog input signal into its single bit digital representation before further signal processing in subsequent digital systems. Depending on how these functions are combined, different architectures can be implemented with different requirements on each function [14]. Figure 1 shows the comparative noise-shaping performance in synchronous and asynchronous modulator architectures. In conventional discrete time modulators, high-frequency noise aliases as in-band noise due to sampling in the loop. Discrete time spectra repeat itself every $f_s/2$. Alternatively, noise is continuous in ASDM. It goes infinite after the switching frequency, but after some harmonics, the spectrum can be neglected.

Continuous Time (CT) synchronous modulators need external clock which has issues like jitter, additional clock generator circuit and so needs additional area and more power. These problems are not present in clockless asynchronous modulator architecture. Amplitude-Time transformation is done with a self-generated limit cycle which avoids quantization noise. The key advantages of asynchronous modulators are: no clock jitter, minimum analog circuits, noise shaping property, and minimum power consumption. Asynchronous circuit implementation also has added benefits of the statistical properties of the input signal such as power spectral density, bandwidth, and maximum signal amplitude [15]. So, we preferred a first order ASDM architecture.

Figure 2 shows the block diagram for first order ASDM architecture which consists of loop filter as CT integrator with ST [6]. Single-loop sigma delta modulators offer an improved stability and linearity [16]. It permits more aggressive noise shaping which results in an improved accuracy and also eliminates the problem of OSR setting compared to synchronous counterparts.

To achieve the field programmability for hysteresis/resolution for the proposed PAM, we improved the ASDM architecture of Fig. 2. This enhanced architecture is shown in Fig. 3. We designed the Operational Transconductance

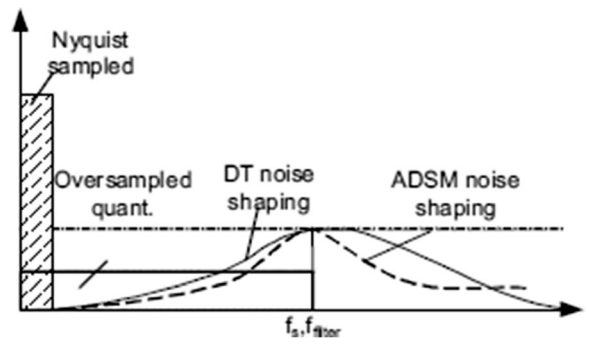


**Fig. 1** Comparison: effect of oversampling, noise shaping in synchronous and asynchronous modulators [28]

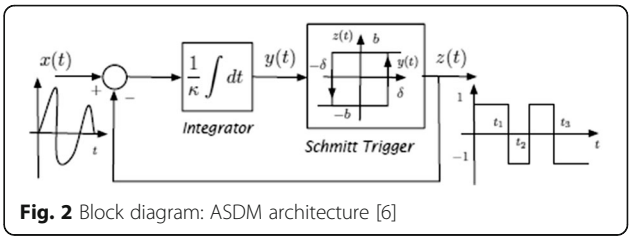


**Fig. 2** Block diagram: ASDM architecture [6]

Amplifier (OTA) integrator and CRST to get programmable hysteresis for resolution control and feedback to get an error signal. This architecture eliminates multiple current sources with switches as in [8, 9] as well-switched capacitor circuits as reported in the various prior literatures. It gives the promise for an efficient performance with power saving. Proposed PAM implementation provides the freedom for adjustment of resolution to the designer for dynamic power optimization. The fundamental principle of operation for the proposed PAM design is discussed in further section.

## 5 Principle of PAM operation

PAM uses a real-time asynchronous mechanism for encoding amplitude information into a time domain; since time can be better resolved, especially in analog low-voltage CMOS circuits. As shown in Fig. 4, quantizer output $z(t)$ switches from low to high if the integrator output rises above the high reference voltage $V_h$ and switches from high to low if the integrator output drops below the low reference voltage $V_l$. The analog signal is losslessly encoded in the transition timings $t_i$. This results in output with varying pulse width and period. The analog pulse width is converted to quantized output $z(t_i)$ as per the duty-cycle modulation principle [17].

Thus PAM converts input signal $x(t)$ to square wave output signal $z(t)$, as per duty-cycle modulation principle [17],

$$\frac{\alpha(t)}{T(t)} = \frac{x(t)+1}{2} \tag{1}$$

Free running frequency takes its maximum value with zero input signal known as the limit cycle frequency (LCF) [17]. For a first-order ASDM, this LCF is defined as [18],

$$f_c = \frac{\pi}{2} f_u \tag{2}$$

where integrator has unity gain frequency $f_u$, which is followed by a CRST with hysteresis $|h|$. With reference to Fig. 2, the amplitude information of the input signal is related to time sequence $t_i \in I$ by [19],

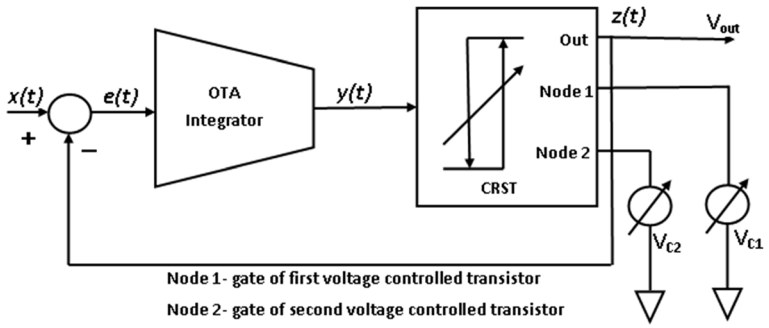


**Fig. 3** PAM architecture: an enhanced ASDM architecture

$$\int_{t_i}^{t_{i+1}} x(t)dt = -1^{i}[-b(t_{i+1}-t_i) + 2\kappa.\delta \quad (3)$$

where $b$, k , and $\delta$ are ASDM parameters. As shown in Fig. 4, time moments $t_i$ related to the zero crossings of $z(t_i)$ coincide with the error signal $e(t)$ crossing the hysteresis values $h$ and $-h$. We used this principle to implement the PAM circuit which is discussed in the next section.

## 6 PAM implementation and analysis

Here, we propose an externally tunable hysteresis controlled PAM as per shown in Fig. 3. *Probably this is the first reported ASDM implementation with external user control; without external current sources and switches.* As in Fig. 3, PAM employs; OTA integrator with bias circuit followed by a CRST with external control voltages. Feedback provides an error signal to the OTA integrator. OTA is preferred as it provides higher gain with improved Input Common Mode Range (ICMR).

*Salient features of this user controlled modulator are:*

(1) Various current sources and switches used in [8, 9] have been replaced by the CRST with field programmability.
(2) If the design uses separate analog and digital power supplies on chip, then one bit feedback DAC can be avoided. So, due to compatibility, there is no need for single-bit feedback DAC.
(3) Noise on the feedback voltages directly subtracts from the input signal and thus improves the modulator's SNDR.
(4) Due to external tuning, it overcomes resolution problems in analog low-voltage CMOS circuits used for ADC.
(5) Field control on resolution and dynamic power consumption is easily possible.

Overall, the proposed design becomes comparatively simple, compact, and efficient with minimum power consumption.

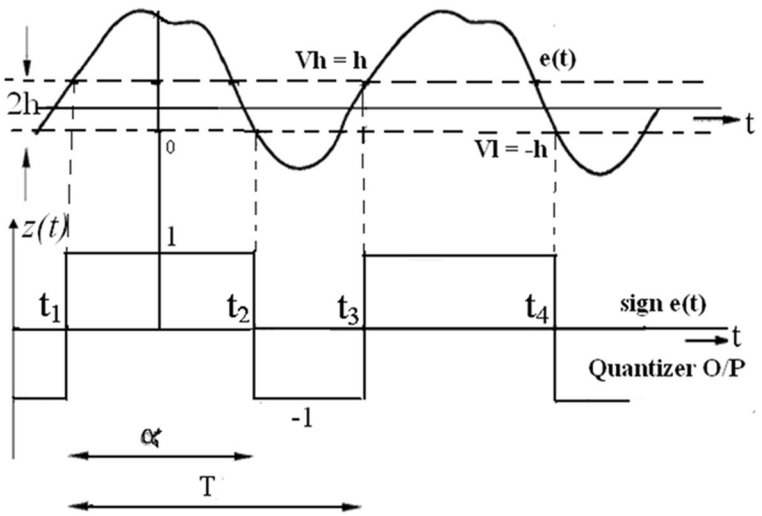


**Fig. 4** Duty cycle modulation principle [19]

Further the proposed PAM design can be realized by analysis for: amplitude-time conversion, upper and lower bounds for pulse width, maximum limit cycle frequency, hysteresis, average limit cycle frequency, modulation depth, and the signal slope.

(a) Amplitude-Time conversion

Input amplitude $x(t_i)$ is converted to time $\alpha_i$ (pulse width), at output as $z(t_i)$ as in Figs. 2, 3, and 4. At any instant $t_i$, the signal on the output of the OTA can be expressed as $y(t_i)$ [19]:

$$y(t_i) = y(t_0) + \frac{1}{\kappa}\int_{t_0}^{t_i}[x(t) - z(t)]dt \tag{4}$$

where $y(t_0)$ represents the OTA output at initial instant $t_0$.

Assume that at this initial instant, CRST is in the state $[y(t_0) = -\delta, z(t_0) = -b]$, and then we can write for $t \geq t_0$:

$$-\delta + \frac{1}{\kappa}\int_{t_0}^{t_i}[x(t) + b]dt = \delta \tag{5}$$

As the signal $y(t_i)$ on the integrator output increases monotonically, the CRST switches to the state $(\delta, b)$ at the instant $t_i = t_1 > t_0$. OTA output $y(t_i)$ can be found on the basis of (4). Subsequently, for $t_i > t_1$:

$$\delta + \frac{1}{\kappa}\int_{t_0}^{t_i}[x(t) + b]dt = -\delta \tag{6}$$

By dividing with $b$ on both sides of (3) and generalizing it, we get [18];

$$\int_{t_i}^{t_{i+1}}\frac{x(t)}{b}dt = (-1)^i\left[-(t_{i+1} - t_i) + \frac{2\kappa.\delta}{b}\right] \tag{7}$$

for all $i, i \in \mathbb{Z}$. Hence, the increasing time sequence $t_i$ can be generated by an equivalent circuit with integration constant $k = 1$ and a CRST with parameters $(\delta/2, 1)$. Thus, modulator uses a simple version without any loss of generality and equation (7) becomes [19]:

$$\int_{t_i}^{t_{i+1}} x(t)dt = (-1)^i[\delta - (t_{i+1} - t_i)] \tag{8}$$

where $\delta$ measured in seconds. Thus, Eq. (8) maps the amplitude information of the signal $x(t_i)$ into the time sequence $z(t_i)$.

(b) Pulse Width: upper and lower bounds

As input is bounded in amplitude by $x(t_i) \leq c$, we can find upper and lower time bounds for CRST output $z(t_i)$. With $x(t) = c$ and $x(t) = -c$ in (5) and (6), respectively, we get [20]:

$$\Delta t_{min} = \frac{2\kappa.\delta}{b + c} \leq (t_{i+1} - t_i) \leq \frac{2\kappa.\delta}{b - c} = \Delta t_{max} \tag{9}$$

The mean signal value $\overline{x}_i$ of the input signal in the $i^{th}$ time window $(t_i, t_{i+1})$ [7]:

$$\overline{x}_i = (-1)^{\mathrm{i}}\left[\frac{2\kappa.\delta}{(t_{i+1} - t_i)} - \mathrm{b}\right] \tag{10}$$

Thus, the amplitude information concerning the mean input signal values $\overline{x}_i$ in exacting time window is encoded in the width of these windows.

(c) Maximum Limit Cycle Frequency (MLCF)

We get maximum frequency in the scheme with zero input. We describe it as a *maximum limit cycle frequency* (MLCF) of the PAM. Equation (9) gives *self-oscillation pulse width* with $c = 0$ [7]:

$$\Delta t_{min} = \Delta t_{max} = \frac{2\kappa.\delta}{b} = T \tag{11}$$

Since, *self-oscillation period* for $z(t)$ is $2T$ and hence MLCF is given by,

$$f_c = \frac{1}{2T} = \frac{b}{4\kappa.\delta} \tag{12}$$

(d) MLCF and hysteresis analysis

The relationship between OTA integrator transfer function $H_L(j\omega)$ and the hysteresis $h$ for a PAM system with input signal $x(t) = 0$ is described by [21]:

$$\frac{4}{\pi}\sum\nolimits_{n=1,3,5}^{\infty}\frac{1}{n}Im\{H_L(jn\omega_c)\} = \pm h \tag{13}$$

The frequency response of an OTA integrator with the characteristic frequency $\omega_p$ is given by:

$$H_L(j\omega) = \frac{1}{j\omega/\omega_p} \tag{14}$$

So expression (13) modifies to:

$$-\frac{4}{\pi}\sum\nolimits_{n=1,3,5}^{\infty}\frac{1}{n}\frac{1}{n\omega_c/\omega_p} = \pm h \tag{15}$$

Hence, $\omega_c$ is given by:

$$\omega_c = \frac{4\omega_p}{\pi h}\sum\nolimits_{n=1,3,5}^{\infty}\left(\frac{1}{n^2}\right) = \frac{4\omega_p}{\pi h}\frac{\pi^2}{8} \tag{16}$$

Substituting $\omega_c = 2\pi f_c$ in (16), we obtain MLCF as:

$$f_c = \frac{\omega_p}{4h} \tag{17}$$

(e) Average Limit Cycle Frequency (ALCF)

Limit cycle frequency alters with the amplitude of the input signal [17]. For a non-zero input signal,

the limit cycle frequency is lower than the value which is given by (17). If a sinusoidal input signal $x(t) = Asin(2\pi f_{in}t)$ is applied, the MLCF as function of time is given as [21]:

$$f_{cs} = \left[1 - A^2 sin^2\left(2\pi f_{in} \cdot t\right)\right] \cdot f_c \tag{18}$$

The Average Limit Cycle Frequency (ALCF) for the sinusoidal signal $x(t)$ is:

$$f_0 = \left(1 - \frac{A^2}{2}\right) \cdot f_c = \left(1 - \frac{A^2}{2}\right) \cdot \left(\frac{\omega_p}{4h}\right) \tag{19}$$

Thus the center frequency shifts as a function of the amplitude of the modulation signal. The ALCF $f_0$ can be reduced by decreasing $\omega_p$ and increasing $h$ as per (17) and (19). The lower limit of $f_0$ should be high enough to keep the frequency components out of the band of interest to avoid degradation of in-band SNR.

(f) Maximum Modulation Depth (MMD)

Maximum Modulation Depth (MMD) of the PAM defined as the ratio of the input signal maximum absolute value $c$ to the amplitude on the PAM output b. The mean modulation depth in $i^{\text{th}}$ time window is the ratio of mean input signal value $\overline{x}_i$ to the amplitude $b$ on the output signal $z(t_i)$. We can rewrite Eq. (9) as [7]:

$$\Delta t_{min} = \frac{T}{1+\eta} \leq (t_{i+1} - t_i) \leq \frac{T}{1-\eta} = \Delta t_{max} \tag{20}$$

$$\text{where : } \eta = c/b; \eta \in [0;1) \text{ and } \eta_i = \bar{x}_i/b \tag{21}$$

(g) Signal Slope: Maximum rate of change of input

Practically, the maximum slope of the input signal needs to be followed by the PAM. The limiting condition for this is:

$$\frac{dV}{dt} = \frac{h}{t_{pd}} \tag{22}$$

where $t_{\text{pd}}$ is the loop propagation time. Setting of $t_{pd}$ is an important design step for a PAM implementation.

Thus for the proposed PAM design implementation, all these analyses are considered. We preferred a use of (12) as a key design parameter. At the start, $f_c$ is set by selecting the design parameters ($k$) for OTA and ($\delta$, $b$) for CRST. Further, (17) and (22) are used for setting of hysteresis level to achieve the programmability. Thus to achieve the control over resolution and dynamic power even after the fabrication, we implemented the novel CRST with external control voltages. Device level implementation with analysis is explained in the following section.

## 7 Circuit design with analysis

Proposed first order PAM includes external control on hysteresis level to adapt the resolution (switching rate). It is preferred to minimize the dynamic power consumption. Number of transitions can be controlled by adjusting step size and thus the control on resolution. Regenerative feedback current can be varied externally to tune the required hysteresis level and thus the step size. We used CRST with external control voltages for this purpose as shown in Fig. 3. Hysteresis has been taken into account in the determination of the system behavior. Overall, the proposed design significantly reduces the analog complexity. This section presents the detail designs of PAM blocks for device level implementations.

A. *Wide-swing folded-cascode OTA*

Integrator leakage limits the gain and increases the inband noise. The slew rate and bandwidth limitations produce harmonic distortion reducing the total SNDR [22]. Integrator determines the overall noise and linearity of the PAM. As this is the critical block due to nonidealities, design should be effective in reducing the inband noise arising from op-amp nonlinearity with low $1/f$ noise and large swing.

The integrator implementations proposed in [8, 9] have been replaced with wide-swing folded-cascode OTA integrator in the present work. To achieve the increased gain, we preferred the use of cascode OTA. Folded topology improves the ICMR with low supply voltage and also offers self compensation, good input common mode range, and the gain of a two stage op-amp [23]. Folded cascode OTA has a good PSSR compared to the two stage op-amp, because OTA is compensated with the load capacitance. A major advantage is positive Common Mode Range (CMR) extends beyond $V_{DD}$ while the negative CMR is limited by minimum voltage across the input differential amplifier. Wide-swing folded-cascode OTA extends CMR up to power supply rails [24]. Hence, we propose wide-swing folded-cascade OTA for this implementation.

The most serious influence of low voltage power supplies on the input stage of the op-amp is ICMR which needs to be set at the center of power supplies. The solution to this problem is to use both n-channel and p-channel differential input stages in parallel. With this topology, minimum value of $V_{DD}$ remains same as for a single differential input stage but gets extended ICMR at the center of power supplies. Thus, it improves ICMR without increasing $V_{DD}$ [23]. We estimated the OTA targets, for the specified

Band-Width (BW) and maximum possible Dynamic Range (DR). We preferred to design the OTA with dc gain up to 70 dB, phase margin below $60^0$ with slew rate 4 V/μs, and DR above 90 dB with maximum SNDR.

Bias circuit (not shown here) is designed for n and p-channel differential stages to provide the widest possible operating range. Bias voltage is applied to the circuit depending on which stage is "ON". Design is implemented for minimum channel lengths with proper biasing currents to achieve the minimum settling time. Figure 5 shows OTA circuit implementation.

An integrator is realized as a first order low-pass filter with the transfer function (14). ALCF increases with characteristic frequency ω of a low pass filter, which further improves the in-band SNR. This is for the reason that the distortion components shift out of the band of interest for higher frequencies.

B. *CRST with varying hysteresis*

As the proposed PAM follows low-frequency signals, the comparator output should reject high-frequency noise variations near the threshold points. Hysteresis is added to the comparator for the performance improvement [23] as shown in Fig. 6b.

Single-ended ST hysteresis is set by device dimensions, process parameters, supply voltage and varies with process conditions [13]. ST with tunable hysteresis overcomes these issues. So, here, we propose use of Current Regenerative Schmitt Trigger (CRST) with external tuning which will allow the control over the PAM performance. CRST circuit implementation is shown in Fig. 7. CRST analysis is discussed below.

$$\text{If} \quad v_{in}^{+} = V_{in} + \Delta V_{in} \quad \text{and} \quad v_{in}^{-} = V_{in} - \Delta V_{in} \tag{23}$$

$$\text{Then} \quad i_{D1} = I_D - \Delta I_D \quad \text{and} \quad i_{D2} = I_D + \Delta I_D \tag{24}$$

where $I_D$ is the current of $M_{1,2}$ when $v_{in}^{+} = v_{in}^{-} = V_{in}$. The increase of $i_{D2}$ will cause the $i_{D3}$ and $i_{D5}$ to rise. Also, the decrease of $i_{D1}$ will cause the $i_{D4}$ and $i_{D6}$ to drop. Because $i_{D3} = (i_{D2} - i_{D6})$ and $i_{D4} = (i_{D1} - i_{D5})$, so $i_{D3}$ will further increase

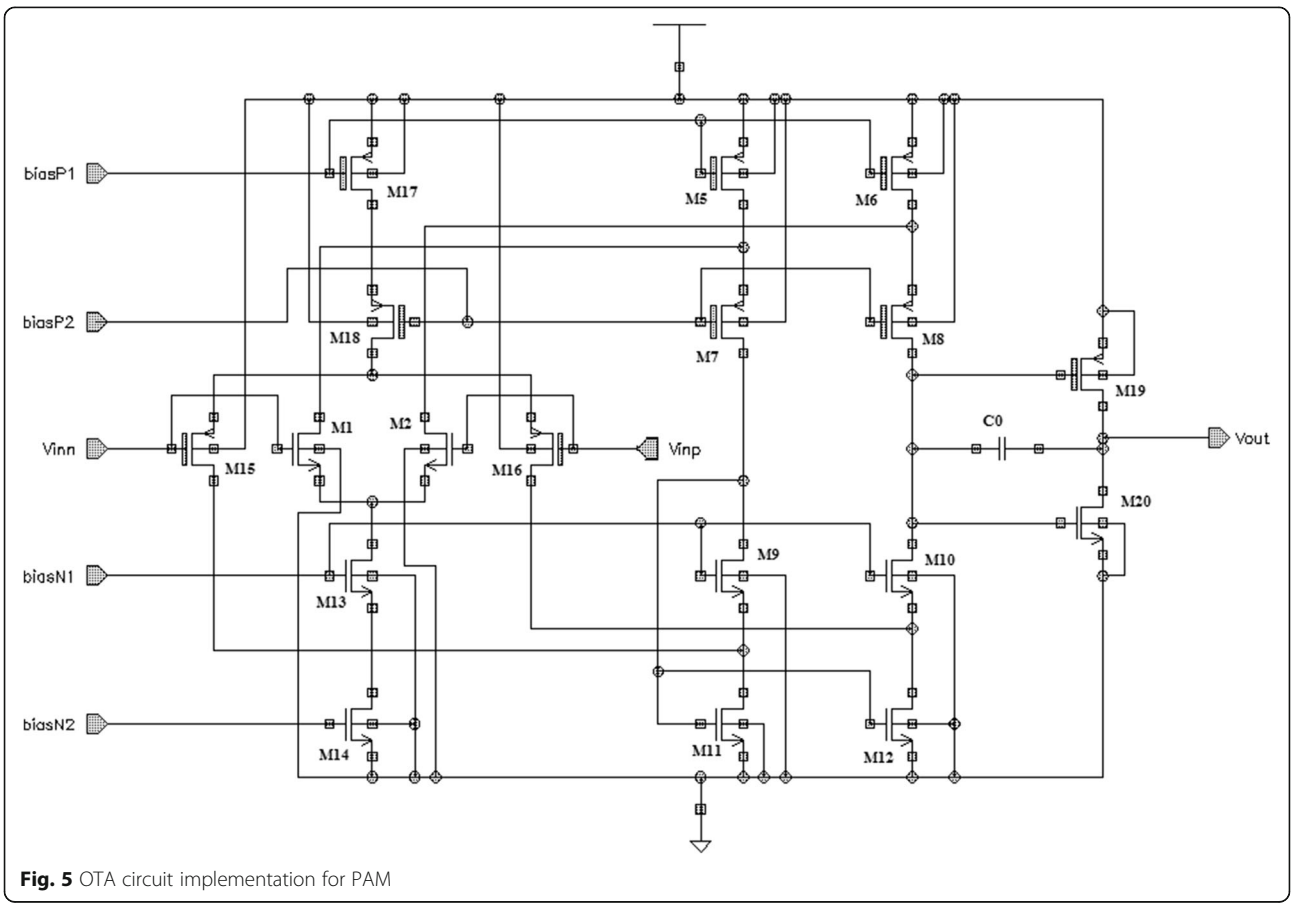


**Fig. 5** OTA circuit implementation for PAM

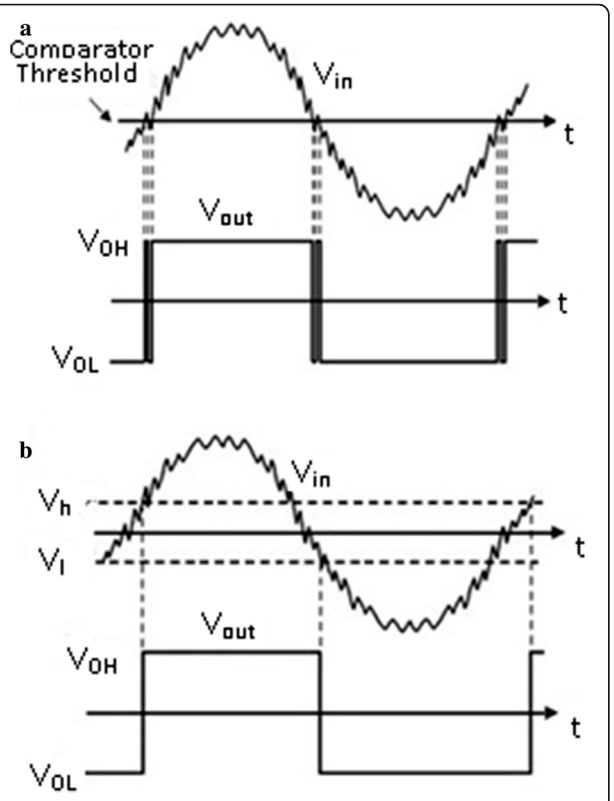


**Fig. 6** **a** Comparator response to a noisy input. **b** Comparator response to a noisy input when hysteresis is added [23]

and $i_{D4}$ will decrease. Thus, the current mirrors $M_{3,5}$ and $M_{5,6}$ provide regenerative current feedback. Since

$$i_{D10} = \frac{(W/L)_{10}(W/L)_7}{(W/L)_9(W/L)_3} i_{D3} \tag{25}$$

$$\text{and} \quad i_{D8} = \frac{(W/L)_8}{(W/L)_4} i_{D4} \tag{26}$$

So, $i_{out} = (i_{D10} - i_{D8})$ increases. This output current will charge the output node capacitor and sets output voltage to logic high (logic 1).

$$\text{Similarly if} \quad v_{in}^{+} = V_{in} - \Delta V_{in} \quad \text{and} \quad v_{in}^{-} = V_{in} + \Delta V_{in} \tag{27}$$

Then, $i_{out}$ will decrease and discharges the output node capacitor to set output voltage to logic low (logic 0). Practically CRST implementation shows three schemes as explained below from [13, 25].

*Scheme I: without regenerative current feedback*

As $i_{D5} = i_{D6} = 0$, we have $i_{D1} = i_{D4}$ and $i_{D2} = i_{D3}$ then [13, 25]:

$$v_{in}^{+} = \left[ v_{in}^{-} + \left( \sqrt{\frac{i_{D3}}{K_2}} - \sqrt{\frac{i_{D4}}{K_1}} \right) \right] \quad \text{where} \quad k_i = \frac{1}{2}\mu_p C_{OX} \left( \frac{W}{L} \right)_i, \quad \text{where } i = 1, 2 \tag{28}$$

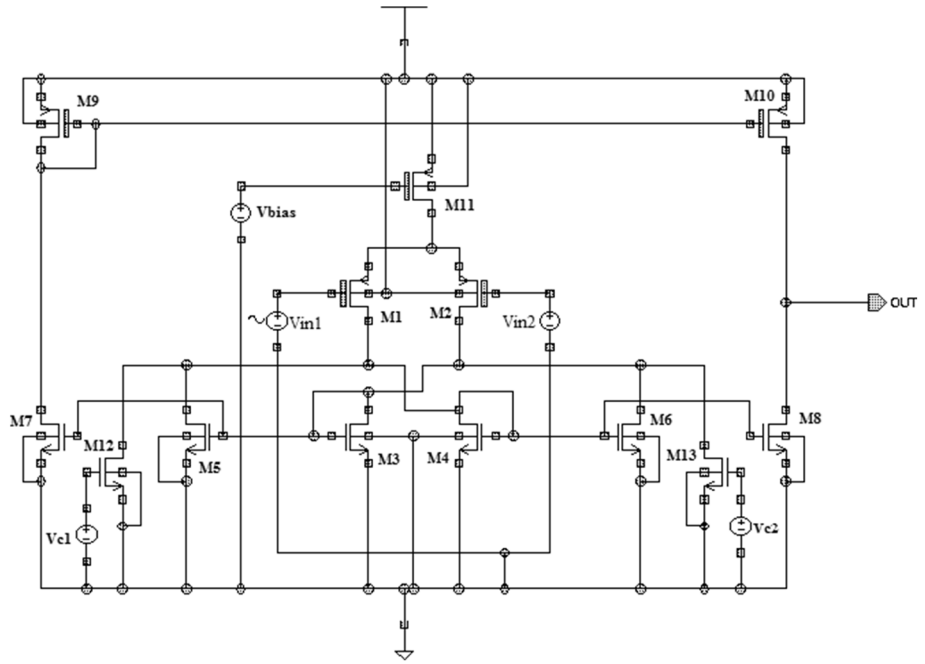


**Fig. 7** CRST circuit implementation for PAM

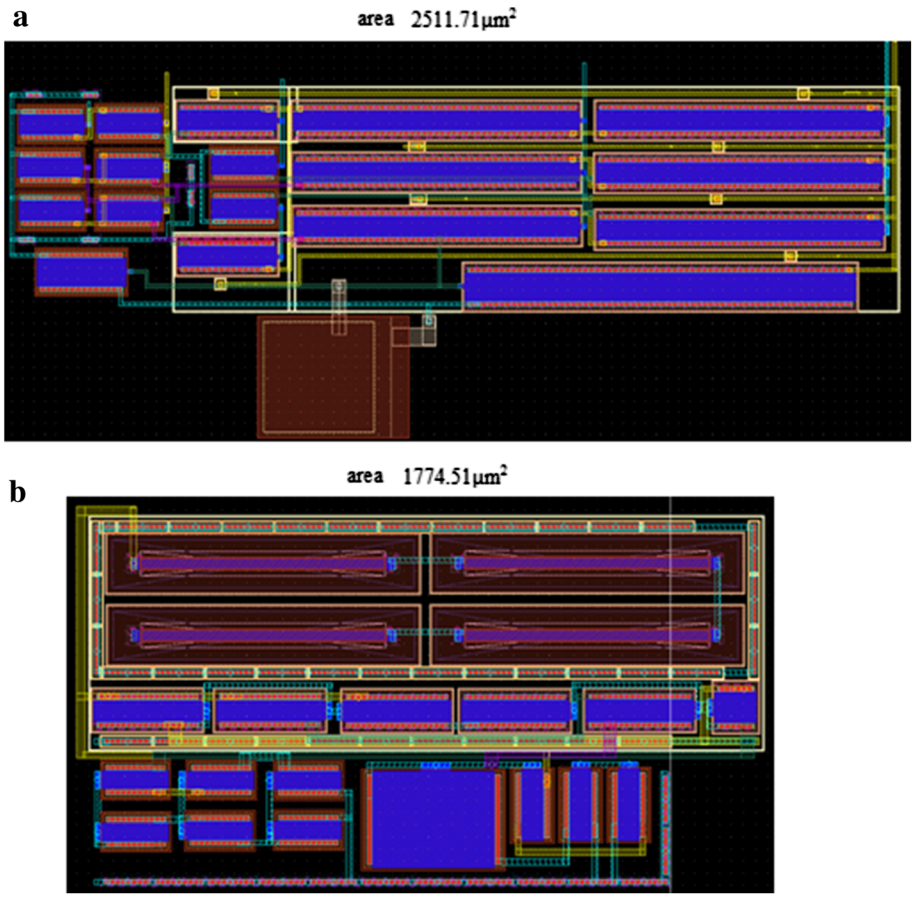


**Fig. 8** Layout design: (**a**) OTA, (**b**) bias circuit

From (28), with $v_{in}^{+} = v_{in}^{-} = v_{in}$ and perfect device matching, i.e., for $k_1 = k_2$ the currents $i_{D3}$ and $i_4$ become equal. It simply shows that with exactly the same input voltages, switching occurs without any regenerative current feedback.

*Scheme II: with regenerative current feedback*

With regenerative current feedback, i.e., if $i_{D5}, i_{D6} \neq 0$, then (28) modifies to [13, 25]:

$$v_{in}^{+} = \left[v_{in}^{-} + \left(\sqrt{\frac{i_{D3}}{k_2}} - \sqrt{\frac{i_{D4}}{k_1}}\right)\right] + \frac{1}{2}\left(\frac{i_{D6}}{i_{D3}}\sqrt{\frac{i_{D3}}{k_2}} - \frac{i_{D5}}{i_{D4}}\sqrt{\frac{i_{D4}}{k_1}}\right) \quad (29)$$

The second term in (29) gives the shift of the switching voltage due to regenerative current feedback. *This shift of the switching voltage gives rise to hysteresis.* Hence, by varying the feedback currents $i_{D5}$ and $i_{D6}$, the hysteresis can be set.

*Scheme III: with variable regenerative current feedback*

In scheme II, the hysteresis can be adjusted by changing the widths of feedback transistors $M_5$ and $M_6$. To make it possible to vary the hysteresis even after fabrication, transistors $M_{12}$ and $M_{13}$ are added as voltage-controlled current sources in parallel

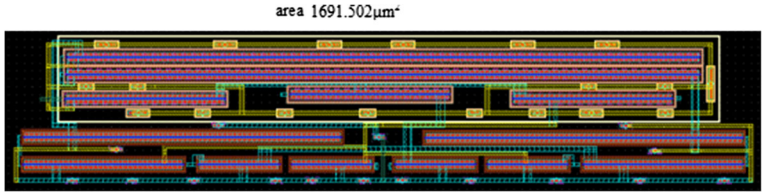


**Fig. 9** CRST layout design

**Table 1** OTA results

| | |
|---|---|
| Gain | 70 dB |
| Bandwidth | 2.2 MHz |
| Phase Margin | $59^0$ |
| Settling Time | 0.91 μs |
| Slew Rate | 3.7 V/μs |

with $M_5$ and $M_6$, respectively, to externally change the currents $i_{D5}$ and $i_{D6}$. Currents through $M_{12}$ and $M_{13}$ are controlled by external voltage sources $V_{c1}$ and $V_{c2}$. This modifies (29) to [13, 25]:

$$v_{in}^{+} = \left[v_{in}^{-} + \left(\sqrt{\frac{i_{D3}}{k_2}} - \sqrt{\frac{i_{D4}}{k_1}}\right)\right] + \frac{1}{2}\left(\frac{i_{D6} + i_{D13}}{i_{D3}}\sqrt{\frac{i_{D3}}{k_2}} - \frac{i_{D5} + i_{D13}}{i_{D4}}\sqrt{\frac{i_{D4}}{k_1}}\right) \quad (30)$$

Thus from (30), it is clear that: simply by varying the control voltages, it is possible to vary the regenerative feedback current and hence the hysteresis. This is the major advantage of the scheme III compared to scheme I and scheme II. Here, we preferred to employ the scheme III for the proposed PAM design, as it offers the freedom of regenerative feedback current programmability. Consequently, the use of CRST, makes it promising to modulate the hysteresis and alternatively control the switching rate of a PAM system for dynamic power saving. CRST implementation for the proposed PAM is shown in Fig. 7.

### C. *PAM implementation*

PAM has been implemented with external hysteresis programmability as shown Fig. 3. The OTA integrator is designed to achieve the maximum possible SNDR. CRST is designed with minimum propagation delay and user flexibility of hysteresis tuning.

Proposed PAM design has been implemented with CMOS analog technology in Cadence Spectre Design Systems with 1.2 V of $V_{DD}$. The designs are analyzed in Virtuoso Analog Design Environment. Layout areas for various blocks are as per OTA in Fig. 8a, bias circuit in Fig. 8b, and CRST in Fig. 9. PAM performance is discussed in the following section.

## 8 Results with discussion

PAM is tested on block and system level with Cadence Virtuso. OTA integrator and CRST blocks are also tested for individual performances. Proposed PAM is tested on system level for pulse width variation, average power performance w.r.t. frequency and hysteresis, SNDR and DR.

*First Block*: Result in Table 1 show that OTA meets the targeted design specifications. Further, OTA has settling time of 0.91 μs which improves the modulator speed. Slew rate and speed is much better than the speed of modulators with switched capacitor implementations in [26, 27].

*Second block*: CRST propagation delay is observed for differential input changes. It shows linear decrease in delay time with increase in differential input. As shown in Fig. 10, linear response is observed till 1.1 V. Further hysteresis width deviation was studied w.r.t. variations in drain

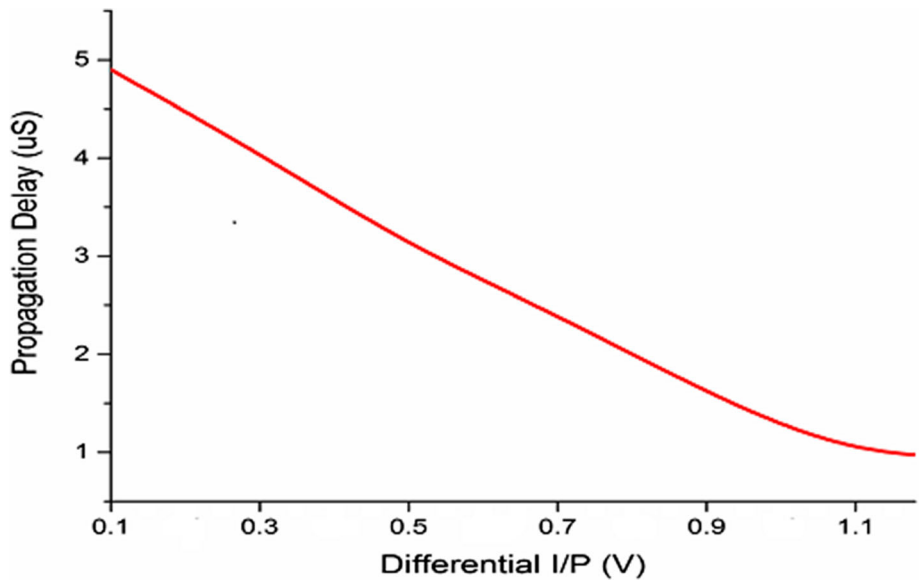


**Fig. 10** CRST propagation delay

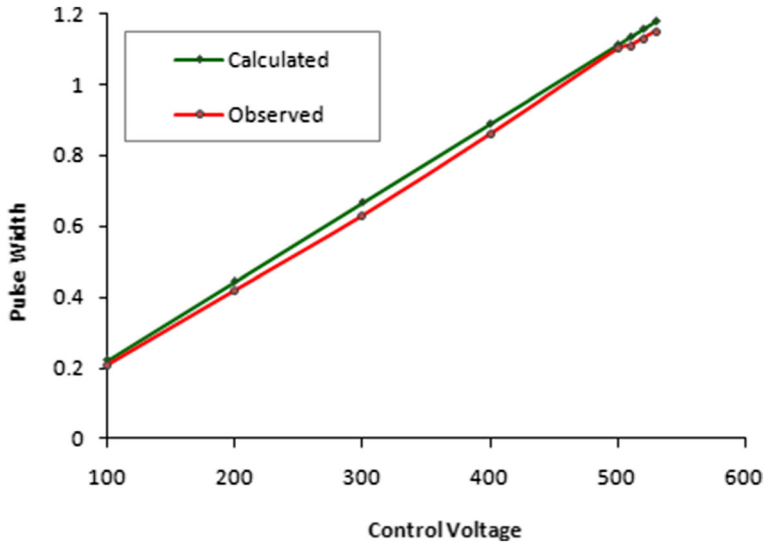


**Fig. 11** Pulse width variation w.r.t control voltage

currents of transistors $M_{12}$ and $M_{13}$ of Fig. 7. Control on these drain currents is through variable control voltages $V_{c1}$ and $V_{c2}$. It is observed that hysteresis width increases with increase in regenerative feedback current. Thus, in particular, CRST hysteresis is the function of the control voltages.

*System level PAM design*: It is characterized by: hysteresis width, signal slope, pulse width $\alpha$, Maximum limit cycle frequency MLCF, power consumption, SNDR, and DR. For the simulation, sinusoidal analog input signal is preferred. PAM converts analog input into single bit digital output.

Figure 11 illustrates the deviation in output pulse width with control voltage variations. Analysis proves the dependence of output pulse width on hysteresis and thus on control voltages. It is also observed that PAM follows the duty cycle modulation principle as (1). Figure 11 shows the example for variation pulse width $\alpha$ with control voltage. It is observed that pulse width $\alpha_i$ varies linearly with control voltage. Using (9) pulse width is calculated and compared with observed pulse width at various control voltages and up to 95 % of $V_{DD}$. Calculated and observed pulse widths are matching for control voltage variation from 100 mV to 600 mV, with 0.15 % error.

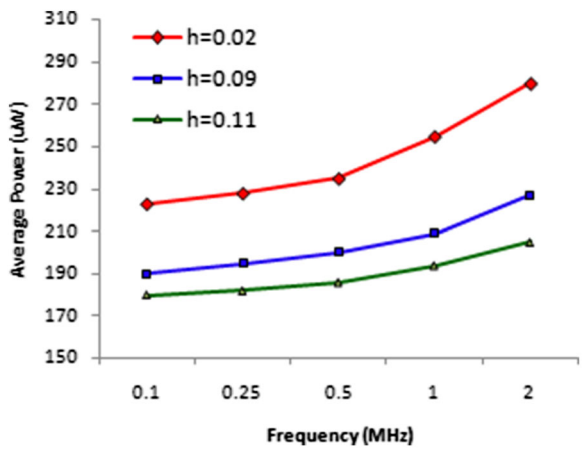


**Fig. 12** Average power verses frequency plots at various hysteresis levels ( h in V )

The PAM average power consumption at various hysteresis levels is shown in Fig. 12. Since the average power consumption is the function of switching rate, the increased input frequency increases the switching activity. It is observed that the power consumption in PAM reduces by average 21 %, over frequency reduction from 2 MHz to 100 KHz. At lower frequencies the switching power reduces due to reduction in effective switching rate. Figure 12 also demonstrates that switching activity can also be reduced by increasing the hysteresis level at any given frequency. By increasing hysteresis from 0.02 to 0.11 V, power reduction of 32 % is obtained at 2 MHz and 24 % is obtained at 100 KHz.

Table 2 illustrates the comparative numerical analysis of the current work with [8, 9] at 2 MHz. Current work relatively shows noticeable power reduction, as the various current sources and the switches are avoided. Figure 13 represents the graphical comparison of a PAM with reference [9], for average power consumption at 1 MHz and

**Table 2** Comparison average power at 2 MHz frequency

| Hysteresis V | Average power consumption (mW) | | |
|---|---|---|---|
| | Ref [8] (0.6 μm) | Ref[9] (0.18 μm) | Current work (0.18 μm) |
| 0.02 | 2.17 | 0.442 | 0.280 |
| 0.09 | 1.8 | 0.304 | 0.230 |
| 0.11 | – | 0.301 | 0.212 |

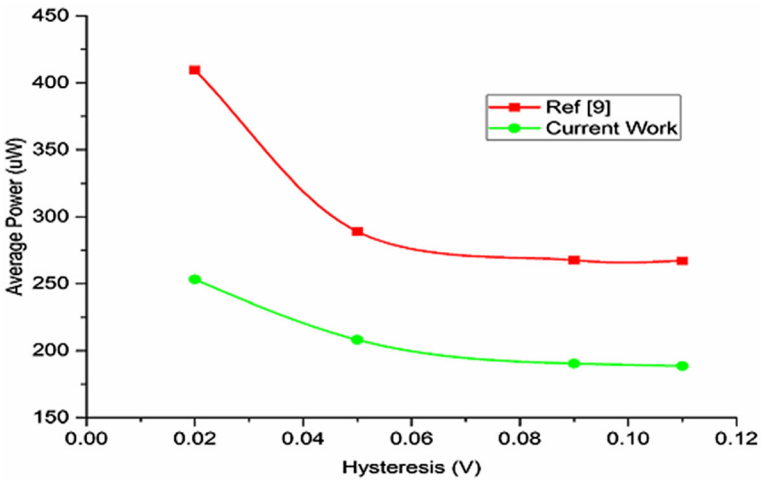


**Fig. 13** Comparison: average power consumption at 1 MHz

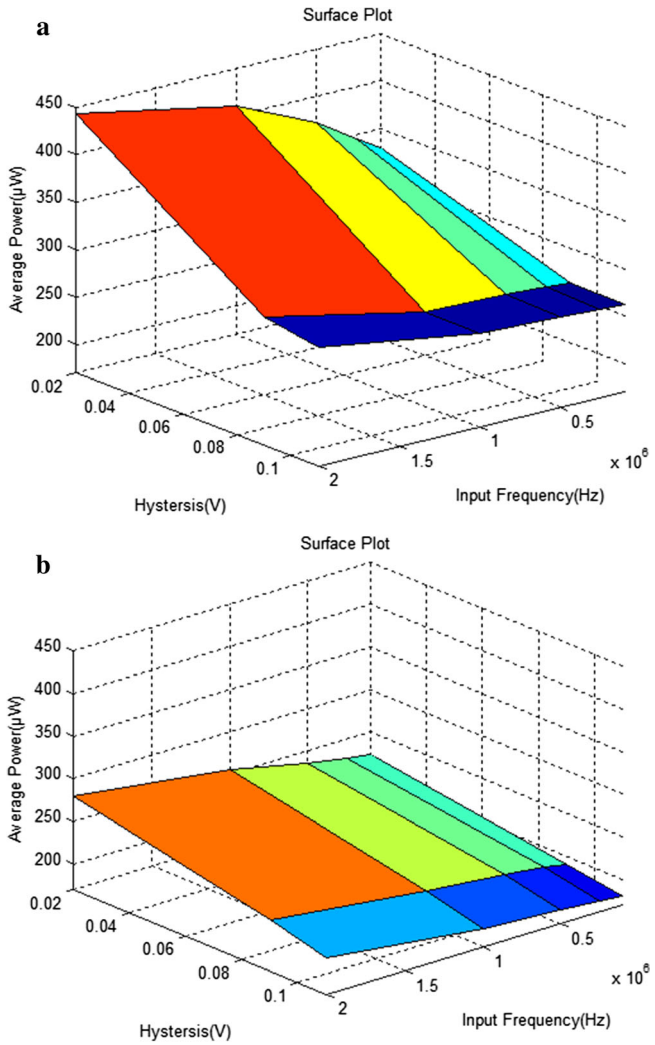


**Fig. 14** Graphical comparison for average power consumption at various frequencies and hysteresis: (**a**) reference [9], (**b**) current work

various hysteresis levels. The proposed design achieves average 30 % power saving as compared to [9]. Relatively average 87 % power reduction was observed with increase in hysteresis from 0.02 to 0.09 V as compared to [8] (0.6 μm technology). Also, 3D graphical representation for average power consumption at various frequencies with hysteresis control is shown in Fig. 14a and b. Noticeable power reduction can be observed with proposed design compared to [9]. It is apparent that PAM power consumption can be controlled by tuning the hysteresis till least possible switching frequency which will result in maximum dynamic power saving. Low-resolution low-power mode is employed for observing the signal. As soon as the activity above threshold is detected, the PAM can be switched to high-resolution high-power mode. Soon after data collection, the PAM can again be switched to low-power low-resolution mode. Maximum power consumption of only 280 μW is observed with proposed PAM implementation.

With the proposed PAM, better SNDR with increased control voltage is achievable because of the enhanced regenerative current. Design [8] achieved the SNR below 30 dB. Comparatively, the proposed PAM attains much higher SNDR. Figure 15 shows the SNDR variation with input amplitude of 2 MHz at various control voltages. It indicates maximum 96 dB DR and 115 dB SNDR. Modulator exhibits Effective Number Of Bits (ENOB) as 18.81 and Figure of Merit (FoM) 0.15 fJ/conversion step.

Thus, the proposed modulator indicates comparatively better design with reduced power and efficient performance. Field programmability for resolution of the modulator is successfully achieved due to the tuning of hysteresis with external control voltages.

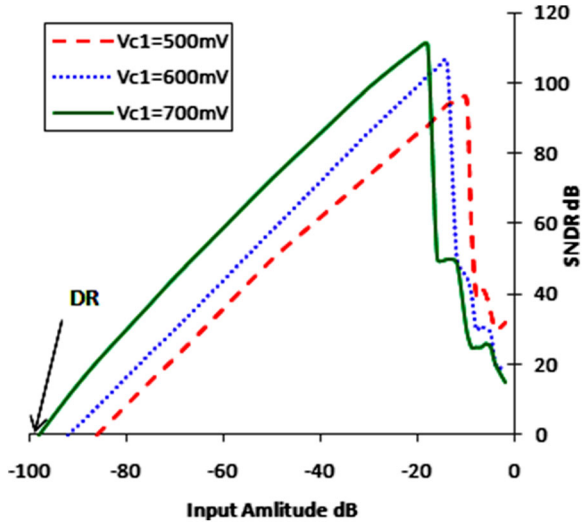


**Fig. 15** SNDR variation with input amplitude at 2 MHz

Consequently, the PAM is useful for the converters demanding better DR with high SNDR and extended battery life.

## 9 Conclusions

The design of resolution/power controllable Asynchronous Sigma-Delta Modulator (ASDM) is successfully presented. Externally variable Current Regenerative Schmitt Trigger (CRST) is used to control the hysteresis, hence the switching rate and the resolution. It is achieved with externally variable control voltages of CRST. It is also possible to set the limit cycle frequency and resolution depending on the input signal slope, without corrupting the inband spectrum. This modulator is novel, as it is able to trade off power with resolution in converters. Proposed optimized Programmable Asynchronous Modulator (PAM) comprehensively reports the field programmability of ASDM. Results proved that the design is compact and power/performance efficient. The proposed improved design is simple yet effective with a new concept implemented for ASDM. It can be a better solution over the sleep-mode circuits with faster wake-up times. Due to its off-chip dynamic power control feature, PAM is attractive for battery-operated IoT devices which uses ADC to achieve power optimization.

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#### Authors' contributions

Concept of resolution/power controllable ASDM is by AAD. Design, implementation and simulation done by AAD under the guidance of RBD. Manuscript written by AAD and editing is done by RBD.

#### Competing interests

The authors declare that they have no competing interests.

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