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*Research Article*

# A Multiplierless DC-Blocker for Single-Bit Sigma-Delta Modulated Signals

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The DC content in single-bit domain is both undesirable and hard to remove. In this paper we propose a single-bit multiplierless DC-blocker structure. The input is assumed to be sigma-delta modulated bitstream. This DC-blocker is designed using a delta modulator topology with a sigma-delta modulator (SDM) embedded in its feedback path. Its performance is investigated in terms of the overall signal-to-noise ratio, the effectiveness of DC removal, and the stability. The proposed structure is efficient for hardware realisation.



## 1. INTRODUCTION

Single-bit systems possess very attractive properties as compared to their multi-bit counterparts. The single-bit implementation produces relatively higher performance and lower hardware complexity. Several relevant previous works have studied and proposed different single-bit structures (e.g., [1–5]). Unfortunately, the design in the single-bit domain has been suffering from two obstacles. First, there are still several unresolved problems such as the adaptivity and stability [6]. Second, the design itself is not straightforward as in multibit techniques. However, we do expect that, ultimately, these pitfalls would be tackled in no far future, and the single-bit or at least the short word-length signal processing (DSP) systems would become very popular [7].

A DC component can be introduced upon a DC-free signal at various stages in the signal bitstream by analog-to-digital conversion or by truncation in fixed-point systems. This DC bias is unwanted in DSP applications as it reduces the dynamic range of the system and can drive the system into saturation. Moreover, a DC-biased bitstream has a highly undesired impact on the performance of the single-bit system, as the DC content bears no information and enhances unwanted limit cycles (which may in turn affect system stability).

In this paper, we propose an efficient single-bit DC-blocker that contains no multi-bit multiplier and would be very simple to be realised using direct hardware implementation or Field programmable gate arrays.

## 2. DESIGN AND ANALYSIS

A simple multi-bit DC-blocker can be seen in [8]. The transfer function of a traditional infinite precision IIR DC-blocking filter is

$$H(z) = \frac{1 - z^{-1}}{1 - \zeta z^{-1}}. \tag{1}$$

The DC cancellation is due to the transfer function having zero at $z = 1$ (0 Hz). The pole at $z = 1 - \zeta$ adjusts the system bandwidth. Our objective is to design a structure that eliminates the DC content which is encoded in single-bit format along with a time-varying input signal. The design of single-bit systems is a nontrivial task. To characterise single-bit systems, it is common to look at both the signal transfer function (STF) and the noise transfer function (NTF) [3]. The STF describes how the modulator alters the original input signal spectrum, and for the DC blocking application, the STF must be a high-pass function. The NTF indicates how effectively the modulator shapes noise spectrum away from the band of interest [9]. The NTF is the main design task which determines the amount of baseband noise shaping performed by the modulator. In general, the NTF is designed to be one of two types: either a pure $M$th-order differentiator, $[\mathrm{NTF}(z) = (1 - z^{-1})^M]$ or a "nonmonotonic"

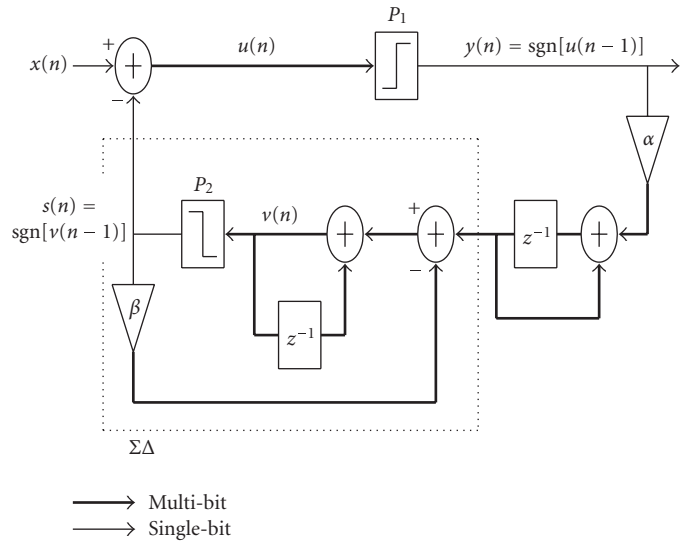


Figure 1: The proposed DC-blocker.

transfer function which has poles in addition to zeros, that is, NTF [NTF$(z) = (z-1)^M/D(z)$]. For either type, as the order $M$ increases, more noise power moves to the unwanted frequency bands, while noise in the wanted frequency bands is reduced. Consequently, signal-to-quantisation-noise ratio (SQNR) in the band of interest is increased [3].

Figure 1 shows the proposed single-bit DC-blocking system. This structure is comprised basically of a delta-modulator structure having a first-order sigma-delta modulator embedded in its feedback loop. We denote the single-bit input by $x(n)$, the bitstream output by $y(n)$, the input to the signal path quantiser $\{\mathrm{P}_1(\cdot)\}$ by $u(n)$, the feedback signal by $s(n)$, and the input to the feedback path quantiser $\{\mathrm{P}_2(\cdot)\}$ by $v(n)$. In this case $y(n)$ and $s(n)$ are given as follows:

$$y(n) = \begin{cases} +1 & \text{for } u(n) \geq 0, \\ -1 & \text{for } u(n) < 0, \end{cases} \tag{2}$$

$$s(n) = \begin{cases} +1 & \text{for } u(n) \geq 0, \\ -1 & \text{for } u(n) < 0. \end{cases} \tag{3}$$

We adopt the well-known linear system approximation approach [10], in which the 1-bit quantisation process is represented by a unity-gain summing element, and the quantisation noise is modelled as an additive, white, and signal-independent noise source with variance $\sigma^2 = \Delta^2/12$ ($\Delta$ represents the quantisation step-size). Let $q_y(n)$ and $q_s(n)$ represent the quantisation noise of the quantisers $\mathrm{P}_1(\cdot)$ and $\mathrm{P}_2(\cdot)$, respectively. It is worth mentioning that the linear model approach is unable to explain many aspects of the SDM behaviour such as integrator spans, stability, limit cycles, and chaos [11]. Nonetheless, the linear approach provides a good approximation to the noise performance of 1-bit systems [12].

Now the transfer function $H(z)$ of the system shown in Figure 1 can be represented as a linear combination of the signal transfer function STF$(z)$ and the noise transfer function NTF$(z)$, that is, $H(z) = \mathrm{STF}(z) + \mathrm{NTF}(z)$. The $z$-transform of the output $Y(z)$ can be described as follows:

$$Y(z) = X(z)\frac{B(z)}{D(z)} + Q_s(z)\frac{z^{-1}(1-z^{-1})^2}{D(z)} + Q_y(z)\frac{B(z)}{D(z)}, \tag{4}$$

where

$$\begin{aligned} B(z) &= (1-z^{-1})[1-(1-\beta)z^{-1}], \\ D(z) &= [1-(2-\beta)z^{-1}+(1-\beta+\alpha)z^{-2}] \end{aligned} \tag{5}$$

with $\alpha$ and $\beta$ are gain parameters. From (4) we have $\mathrm{STF}(z) = B(z)/D(z)$, whereas two separate noise-shaping functions are in effect: $\mathrm{NTF}_s(z) = z^{-1}(1-z^{-1})^2/D(z)$ and $\mathrm{NTF}_y(z) = B(z)/D(z)$. These noise-shaping functions will high-pass filter the quantisation noise processes $Q_s$ and $Q_y$, respectively.

In order to remove the DC content from the input bitstream, the STF of the system should operate as a high-pass filter. Based on (4), Figure 2 depicts the theoretical frequency response curves of $\mathrm{STF}(e^{j\Omega})$ and $\mathrm{NTF}_y(e^{j\Omega})$.

It is obvious from (4) that the system function, $Y(z)$, contains two zeros $z_{1,2}$ and two poles $p_{1,2}$ as follows:

$$z_1 = 1, \qquad z_2 = 1-\beta, \tag{6}$$

$$p_{1,2} = (1-0.5\beta) \mp \sqrt{(1-0.5\beta)^2 - (1-\beta+\alpha)}. \tag{7}$$

The above poles will take real values for $\beta \geq 2\sqrt{\alpha}$ and form a conjugate pair when $\beta < 2\sqrt{\alpha}$. The gain parameters $\alpha$ and $\beta$ play an important role in characterising the performance of the DC-blocker through the control of pole-zero locations. Accordingly, their combination will specify the system bandwidth. However, it should be noted that for $\alpha = 0$, the two poles occupy the locations of the two zeros, and hence cancel each other. For that $\alpha$ is the critical parameter in this regard, as its value determines how much the poles and zeros are separated.

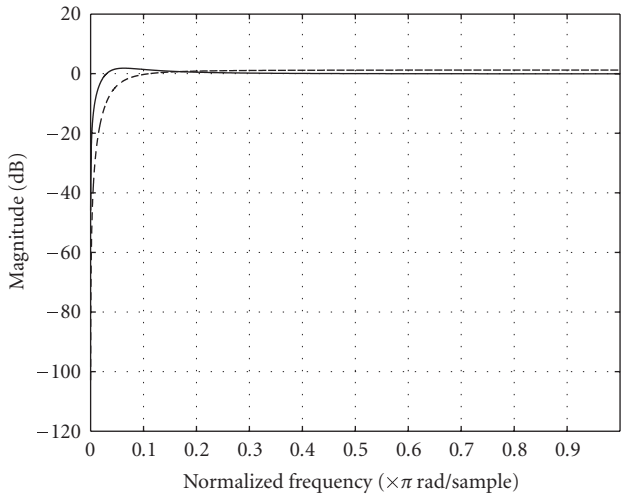


FIGURE 2: Signal and noise transfer functions, $\mathrm{STF}(e^{j\Omega})$ and $\mathrm{NTF}_y(e^{j\Omega})$, of the DC-blocker using first-order SDM with $\alpha = 0.0205$ and $\beta = 0.2705$.

The performance of the proposed structure can be evaluated in terms of the overall signal-to-noise ratio (in the band of interest) plus the signal-to-quantisation-noise ratio, $\mathrm{SNR}_{\mathrm{ov}}$. From (4), $\mathrm{SNR}_{\mathrm{ov}}$ can be calculated as [13, 14]

$$\mathrm{SNR}_{\mathrm{ov}} = \int_{-\Omega_B}^{\Omega_B} \left| \frac{X(e^{j\Omega})\,\mathrm{STF}(e^{j\Omega})}{G(e^{j\Omega})} \right|^2 d\Omega, \tag{8}$$

where $\Omega_B \in (0, \pi)$ denotes the normalised desired signal bandwidth ($\Omega = \pi$ corresponds to half the sampling rate, $\Omega_s$) and $G(e^{j\Omega})$ is given by

$$G(e^{j\Omega}) = Q_y(e^{j\Omega})\,\mathrm{NTF}_y(e^{j\Omega}) + Q_s(e^{j\Omega})\,\mathrm{NTF}_s(e^{j\Omega}). \tag{9}$$

Note that $X(e^{j\Omega})$ represents the input bitstream spectrum, assumed to contain quantisation noise as a result of a previous SDM encoding process in addition to white Gaussian noise.

## 3. SIMULATION AND DISCUSSION

MATLAB is utilised to simulate the proposed structure. We denote by $\mathrm{SNR}_{\mathrm{ovi}}$ the overall input SNR. To meet the standard audio specifications, we suggest $\mathrm{SNR}_{\mathrm{ovi}} = 20$ dB. To assess the performance of the DC-blocker, we define the parameter $\rho = 10\log_{10}(\mathrm{SNR}_{\mathrm{ovo}}/\mathrm{SNR}_{\mathrm{ovi}})$, where $\mathrm{SNR}_{\mathrm{ovo}}$ stands for the output $\mathrm{SNR}_{\mathrm{ov}}$. The optimal values for the gain parameters $\alpha$ and $\beta$ are specified in the sense of maximum attainable $\mathrm{SNR}_{\mathrm{ovo}}$, that is, maximum $\rho$ (or $\rho_m$). Figure 3 illustrates $\rho$ as a function of the gain parameters $\alpha$ and $\beta$ such that both span the interval $(0, 0.1]$ in a step-size of $2^{-10}$. Simulation shows that the optimum operating point $\rho_m(\alpha_m, \beta_m)$ for the DC-blocker in Figure 1 occurs when $\alpha_m = 0.0205$ and $\beta_m = 0.2705$ such that maximum $\rho$ equals about $-1.51$ dB. The resolution of the multi-bit region in the DC-blocker is assumed to be 10-bit in this simulation. The resolution can be changed according to the application requirements.

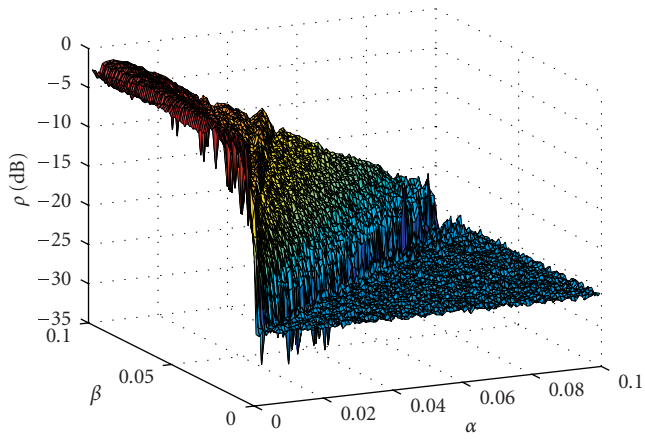


FIGURE 3: The ratio $\rho = \mathrm{SNR}_{\mathrm{ovo}}/\mathrm{SNR}_{\mathrm{ovi}}$ (in dB) versus the gain parameters $\alpha$ and $\beta$ using 10-bit resolution.

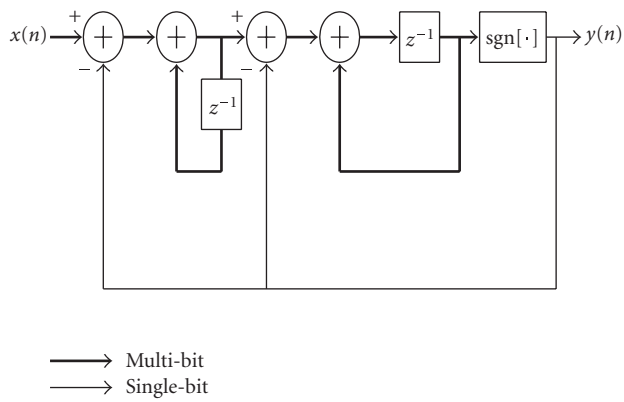


FIGURE 4: Block diagram of second-order sigma-delta modulator.

The degradation in $\mathrm{SNR}_{\mathrm{ovo}}$ can be removed by replacing the first-order SDM in the feedback path of the DC-blocker with a higher-order one as shown in Figure 4. Figure 5 depicts the improvement in $\rho_m$ when a second-order SDM stage is embedded in the proposed structure. In this case $\rho_m = 3.6$ dB for $\alpha_m = 0.0127$ and $\beta_m = 0.0508$, where significant improvement in the performance is achieved over the first-order SDM-based DC-blocker.

A comparison between the simulated frequency response curves of the DC-blocker for first- and second-order SDM stages for optimum $\rho$ is depicted in Figure 6. The dashed vertical lines indicate the desired signal band for OSR = 32.

In Figure 7, the input and output spectra of the DC-blocker with second-order SDM are shown. It is evident that the DC component in the input signal is removed. Moreover, an improvement in the SNR of more than 2 dB is obtained. The input is taken as $A_{\mathrm{DC}} + A\sin(\omega_o t) + n(t)$, where $A_{\mathrm{DC}} = 0.5$, $A = 0.5$, $\omega_o = 8192\pi$ rad/s (chosen to be in the audio band), and $n(t)$ is an additive white Gaussian noise (AWGN) process. Hence, the input signal contains a DC component that is twice in magnitude as the sinusoidal component. To meet the minimum requirement for audio applications, the

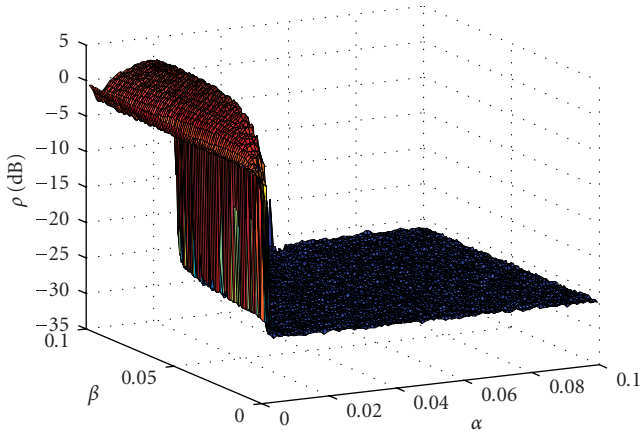


Figure 5: The ratio $\rho$ versus the gain parameters $\alpha$ and $\beta$ (10-bit resolution) of the DC-blocker using a second-order SDM.

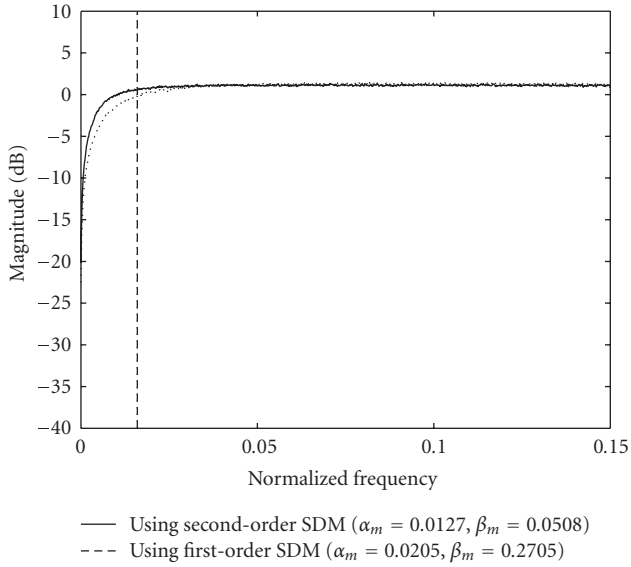


Figure 6: Frequency response of the simulated DC-blocker: (solid) using second-order SDM ($\alpha_m = 0.0127$, $\beta_m = 0.0508$); (dotted) using first-order SDM ($\alpha_m = 0.0205$, $\beta_m = 0.2705$).

overall signal-to-noise ratio ($SNR_{ovi}$) is made as 20 dB. Different input types have also been used in this test, including sawtooth, FM, and AM-FM signals. In all cases, the response curves are comparable to those shown for the sinusoidal input, as can be seen in Figure 8 for FM input.

From hardware implementation viewpoint, the proposed DC-blocker is very simple, as it contains no multi-bit multipliers. The gain parameters $\alpha$ and $\beta$ can be realised using simple digital scalers. For FPGA implementation, these two gains can be achieved by using two multiplexers, each of them multiplexes two fixed multi-bit numbers (that represent $\alpha$ and -$\alpha$ or $\beta$ and -$\beta$), where the multiplexer output is dependent on the quantiser output as shown in Figure 9.

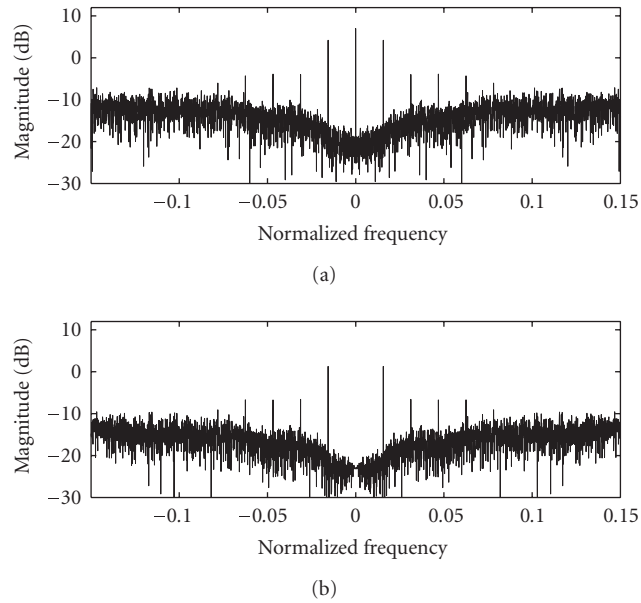


Figure 7: Input and output spectra of the DC-blocker (using a second-order SDM) for a sinusoidal input.

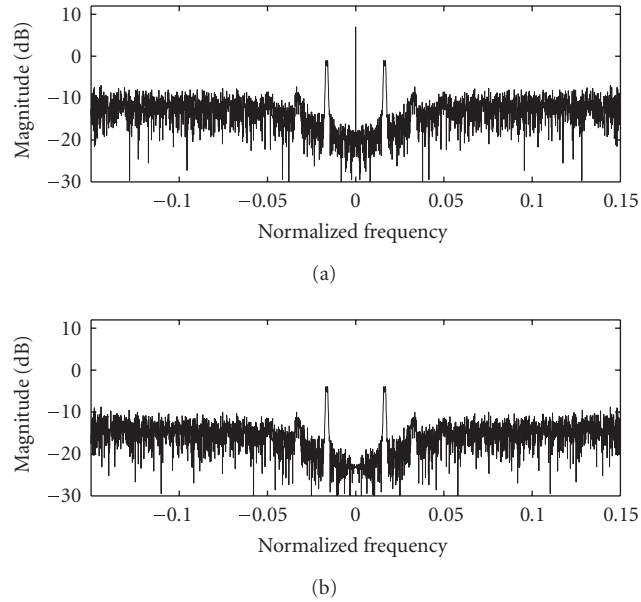


Figure 8: Input and output spectra of the DC-blocker (using a second-order SDM) for an FM input.

## 4. STABILITY

The proposed structure is a linear system except for the single-bit quantisers which are nonlinear elements. As mentioned earlier, using linear approximation is inadequate to model this system accurately. However, the linear model does reveal some valuable analytical results when using a low order ($\leq 2$) SDM stage in the feedback loop. The stability problem would be complicated when using a third- (or higher-)

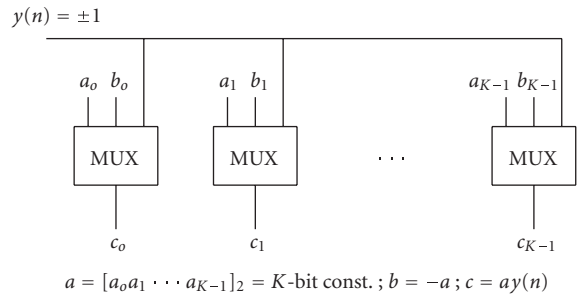


Figure 9: Multiplication of a single-bit signal by a multi-bit constant.

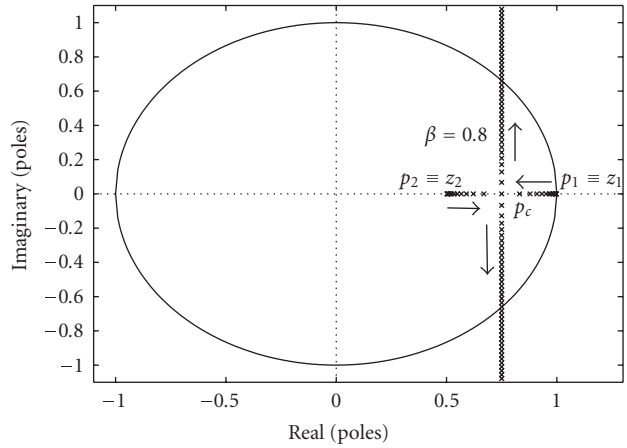


Figure 10: Root-locus of the proposed DC-blocker with $\beta = 0.8$.

order SDM, as these high-order topologies are prone to the instability problem [15]. A detailed nonlinear stability analysis is beyond the scope of this paper, however, investigating the root-locus of the system would be useful to approximate its stability criteria.

Considering the system with first-order SDM as shown in Figure 1 with zeros and poles as given by (6) and (7), the parameter $\beta$ determines the locations of one zero ($z_2$) and the two poles $p_{1,2}$ (noting that for $\alpha = 0$, zeros and poles will cancel each other), while $\alpha$ controls the pole-zero separation in each pole-zero pair. Figure 10 can be used to clarify the root-locus behaviour of this system as follows when $\beta = 0.8$. Starting with $\alpha = 0$, each pole will occupy (cancel) a zero, that is, $p_1 = z_1 = 1$ and $p_2 = z_2 = 1 - \beta$. The distance between these two initial poles is $\beta$. Let the mid point between the two initial poles be represented by $p_c$, then $p_c = 0.5(p_1 + p_2) = 1 - 0.5\beta$. As $\alpha$ increases, the two poles will travel horizontally in opposite directions on the real axis until they meet at $p_c$ when $\alpha = (0.5\beta)^2$. The point $p_c$ will remain as mid point between the two poles as they move. Further increase in $\alpha$ beyond $(0.5\beta)^2$ will drive the two poles to be a complex conjugate pair tracing a vertical line centered at $p_c$ (with the right pole moves upwards, while the other moves downwards). The intersection points between the unit circle and this vertical line will reveal the stability criteria of the

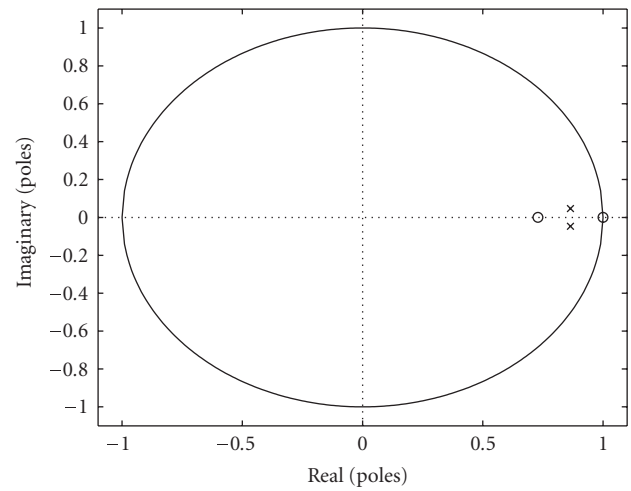


Figure 11: Pole-zero plot of the DC-blocker with first-order SDM at $\rho = \rho_m$ using $\alpha = 0.0205$ and $\beta = 0.2705$.

system. Denoting the real axis as $\mu$ and the imaginary axis as $\nu$, any intersection point satisfies the relation

$$\nu = \sqrt{\beta - \frac{\beta^2}{4}}. \tag{10}$$

Moreover, the poles in equation (7) will give

$$\left| \left(1 - \frac{\beta}{2}\right) \mp \sqrt{\left(1 - \frac{\beta}{2}\right)^2 - (1 - \beta + \alpha)} \right| = 1. \tag{11}$$

Now using (10) and (11), the following conditions for the complex conjugate poles can be reached:

$$\left(\frac{\beta}{2}\right)^2 < \alpha < \beta < 2 \tag{12}$$

while for real poles the following conditions are obtained:

$$\alpha < \min\left\{\left(\frac{\beta}{2}\right)^2, \beta\right\}; \qquad \beta < 2 \tag{13}$$

which can be reduced to

$$\alpha < \left(\frac{\beta}{2}\right)^2 < 1. \tag{14}$$

The poles will exit the unit circle circumference if $\alpha > \beta$.

Figure 11 shows the pole-zero plot of the system shown in Figure 1 at the optimum operating point $\rho = \rho_m$, with $\alpha = 0.0205$ and $\beta = 0.2705$. From an LTI system viewpoint, this plot confirms that the designed DC-blocker is always stable. This is so because all poles are located within the unit circle in the $z$-domain. However, since our system is nonlinear, this condition from linear analysis is considered sufficient for stability but not necessary [16]. Simulation results confirm this claim.

## 5. CONCLUSION

A single-bit multiplierless DC-blocker is proposed. The structure is comprised of a delta-modulator structure with a sigma-delta modulating (SDM) stage in its feedback loop. The proposed system is evaluated in terms of the overall SNR and the magnitude of DC attenuation. It is shown that using a second-order SDM improves the overall system SNR as compared to using a first-order one. However, using higher-order SDM (> 2) would complicate the stability issue as higher-order SDM topologies inherently suffer from instability problem. The role of the gain parameters is investigated and optimal performance has been reached assuming 10-bit resolution. Stability criteria have been derived. The system is examined using different types of signals. The proposed DC-blocker is very efficient for FPGA hardware realisation.

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**Zahir M. Hussain** took the first rank in Iraq in the General Baccalaureate Examinations 1979 with an average of 99%. He received the B.S. and M.S. degrees in electrical engineering from the University of Baghdad in 1983 and 1989, respectively, and the Ph.D. degree from Queensland University of Technology, Brisbane, Australia, in 2002. From 1989 to 1998 he lectured on electrical engineering and mathematics. In 2001 he joined the School of Electrical and Computer Engineering, RMIT University, Melbourne, Australia, as a researcher then lecturer of signal processing and academic leader of a 3G commercial communications project. In 2002 he was promoted to Senior Lecturer. He has been the senior supervisor for nine Ph.D. students at RMIT. Dr. Hussain has over 120 technical publications on signal processing, communications, electronics, and mathematics. His joint work with Dr. Peter O'Shea on single-bit processing has recently led to an ARC Discovery grant. In 2005 he was promoted to Associate Professor and got RMIT 2005 Publications Award. He is currently the Head of the Communication Engineering Discipline at RMIT. Dr. Hussain is a member of Engineers Australia, IEE, and a senior member of IEEE. He is a reviewer for many IEEE and Elsevier Journals.

**Peter O′Shea** received the B.E., Dip.Ed., and Ph.D. degrees all from the University of Queensland. He has worked as an engineer at the Overseas Telecommunications Commission for 3 years, at University of Queensland for 4 years, at Royal Melbourne Institute of Technology (RMIT) for 7 years, and at Queensland University of Technology (QUT) for 9 years. He has received awards in Student Centred Teaching from the Faculty of Engineering and the University President at both RMIT and QUT. His interests are in signal processing for communications, power systems and biomedicine, and in reconfigurable computing.