

# An Analog Correlator for Ultra-Wideband Receivers

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We present a new analog circuit exhibiting high bandwidth and low distortion, specially designed for signal correlation in an ultra-wideband receiver front end. The ultra-wideband short impulse signals are correlated with a local pulse template by the correlator. A comparator then samples the output for signal detection. A typical Gilbert mixer core is adopted for multiplication of broadband signals up to 10 GHz. As a result of synchronization of the received signal and the local template, the output voltage level after integration and sampling can reach up to 100 mV, which is sufficient for detection by the comparator. The circuit dissipates about 30 mW from double voltage supplies of 4 V and 4.4 V using 0.24  $\mu\text{m}$  SiGe BiCMOS technology. Simulation results are presented to show the feasibility of this circuit design for use in ultra-wideband receivers.

**Keywords and phrases:** analog correlator, Gilbert cell, ultra-wideband receiver.

## 1. INTRODUCTION

Ultra-wideband (UWB) communication systems have been drawing increasing attention in recent years due to their attractive features of high transmission rates and low cost. UWB systems transmit information through short impulses, in contrast to traditional wireless communication systems, which use sinusoidal carriers.

In impulse radio systems, several modulation techniques may be deployed including pulse position modulation (PPM) and pulse amplitude modulation (PAM) [1], for all of which a correlator is an indispensable component for detection by the receiver [2]. In order to lower the cost and power of wireless mobile devices, it is necessary to integrate UWB systems on a single chip, thereby enabling a wide range of applications in the wireless data communication field. This process represents a big challenge for current VLSI technology, because of the UWB range involved from 3.1 GHz to 10.3 GHz. At present, only a few publications dealing with this topic have therefore been published. An integrated UWB transceiver architecture for low data rates (100 Kbps) at low bandwidth (below 960 MHz) using a digital implementation of the correlator has been described in [3]. Although a correlator can also be implemented in digital format for high

data rates of up to 100 Mbps at high bandwidth, direct sampling of 3.1 GHz to 10.3 GHz frequency signals is ultimately required, which is almost impossible for current ADC techniques. The advantage of an analog correlator is that it can process signals in real time and provide a continuous output at low frequency, and thereby can remove the need for special requirements for the ADC in the receiver. Analog correlators are therefore well suited for UWB front-end implementation. Although some authors [4] have presented a multiple correlator implementation, no details have yet been presented.

The correlator is one of the key parts of the receiver front-end, which also includes a low-noise amplifier (LNA) and a comparator [5], as shown in Figure 1. The received signal is correlated with the local template impulse during a certain period, normally the pulse repetition period or the symbol period, and its output is sampled and held to detect whether there is a signal in the observing window.

A new 3–10 GHz analog correlator, composed of a standard Gilbert cell (GC) [6], a load capacitor, and other supporting circuits, is proposed in this paper. The standard GC multiplies the received signal with the template, and then the product is integrated by the load capacitor. In order to evaluate the performance of the correlator, a two-tone model is also described.

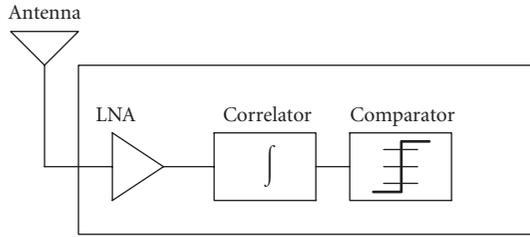


FIGURE 1: Receiver front-end block diagram.

The paper is organized as follows. In Section 2, the principles behind the correlator design are described. Results of some simulations concerning the correlator performance are then analyzed in Section 3. Finally in Section 4, we present our conclusions.

## 2. CORRELATOR DESIGN

A correlator is used to detect the presence of signals with a known waveform in a noisy background. The output is nearly zero if only noise is present [2]; otherwise, the energy of the received signal is integrated with the local template waveform for a certain time interval to obtain a high-voltage output above the a predefined threshold. The cross-correlation function can be described by the following equation:

$$f = \int_{t=t_0}^{t=t_0+T} \text{RF}(t) \text{LO}(t) dt, \quad (1)$$

where  $\text{LO}(t)$  is the local template signal,  $\text{RF}(t)$  is the input radio frequency signal of the correlator, and  $T$  is the integration period.

The correlation process can be divided into two steps. The first step involves multiplication of the received signal and the reference waveform (local template signal) using a standard GC. The second step involves integration of the output current via a capacitor. The basic correlator topology is depicted in Figure 2. The standard GC, as a current-mode element, outputs the differential current. The typical resistive or inductive load of a standard Gilbert mixer is replaced by two current sources and a capacitor across the differential output nodes. Because the common-mode part of the output current is absorbed by the current source load, the differential output current is directly fed into the load capacitor. As a result, the capacitor integrates the current and outputs a step-like voltage. A switch controlled by an external clock is used to determine the integration interval, and to clear the charge in the capacitor at the end of each interval.

The circuit described in this paper is based on SiGe BiCMOS technology. This technology, intended for RF, analog, and mixed signal applications, has high-performance graded-bandgap-base negative-positive-negative (NPN) transistors, integrated with high-density complementary metal-oxide semiconductor (CMOS) logic. The minimum lithographic image length is  $0.24 \mu\text{m}$ ; the transient frequency

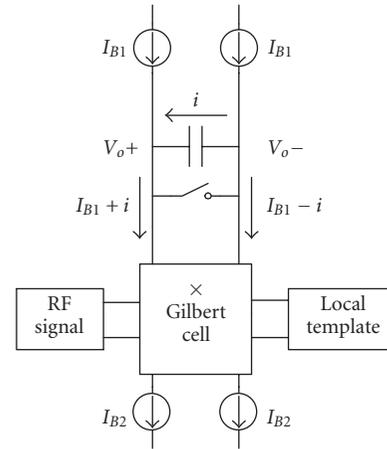


FIGURE 2: Correlator topology.

$f_t$  of the standard NPN transistor is 47 GHz. Figure 3 gives a schematic of the circuit design, which consists of three parts: a predistortion circuit (PDC), a GC, and a common-mode feedback (CMFB). The values of  $R_1$  and  $I_E$  are chosen as  $10 \Omega$  and  $2 \text{mA}$ , respectively, as a tradeoff between linearity and the transconductance of the PDC. The emitter areas of  $Q_1$  and  $Q_2$  are chosen to be as small as possible, in order to increase the differential voltage  $V_p$ . The GC ( $Q_5$ – $Q_{10}$ ) multiplies the predistorted template  $V_p$  with the received pulses (RF signal), and then outputs the product in differential current mode. The GC is implemented using bipolar transistors for the following two reasons. The first reason is that high-speed multiplication is required, and bipolar transistors have a higher transient frequency than metal-oxide semiconductor (MOS) transistors. The second reason is that a GC in a bipolar form has better linearity than that deployed in MOS transistors, allowing better compatibility with the PDC.  $R_2$  helps to transform the template voltage to current in a more linear manner.  $M'_1$ – $M'_4$ ,  $M_1$ – $M_4$ , and  $Q_{11}$ – $Q_{14}$  are current sources, which supply bias currents for the GC and CMFB circuits. Because an active load is used, it is necessary also to add a CMFB circuit to determine the output common-mode voltage and to control this voltage to be equal to a specified value  $V_{CM}$ . The CMFB circuit includes  $M_5$ – $M_8$  and  $Q_{13}$ – $Q_{14}$ . The values of  $M_5$ – $M_8$ ,  $Q_{11}$ – $Q_{14}$ ,  $M_1$ – $M_4$ , and  $M'_1$ – $M'_4$  are matched, so that the output common-mode voltage should be equal to  $V_{CM}$  under steady-state conditions, with transistors  $M_5$ – $M_8$  operating in the triode region [6]. In practice the base currents of  $Q_5$ – $Q_{12}$  cannot be neglected, therefore the current “above” the GC ( $I_{B1}$  in Figure 2) is not exactly equal to the current “below” it ( $I_{B2}$  in Figure 2). Because the correlator and LNA are integrated in the same chip, port impedance matching is not considered here.

## 3. SIMULATION RESULTS

The circuit shown in Figure 3 has been simulated using Cadence Spectre with the Gummel-Poon NPN model and the

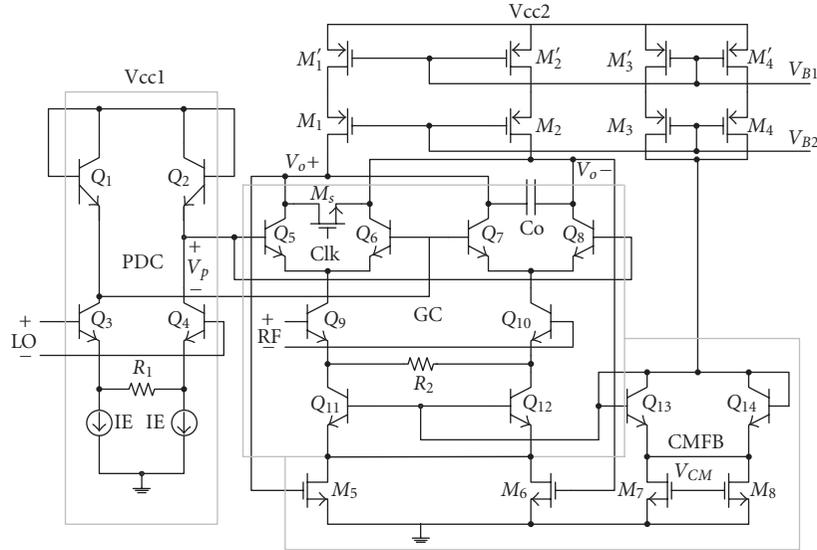


FIGURE 3: Schematic of the correlator.

BSIM3v3.2 intrinsic MOSFET model presented by IBM. In the following, some selected simulation results are shown and analyzed.

### 3.1. Correlator characteristics

We have chosen to describe the correlator characteristics in the frequency domain. There are two reasons for this choice.

- (1) In current EDA simulation systems, frequency-domain simulation techniques are the most popular, and provide an effective way to describe and control the behavior of a circuit, especially for frequency translation circuits.
- (2) For testing a RF circuit, tones of specified frequency are more easily available than short pulses in a time domain.

The behavior of a correlator can be described in the frequency domain as

$$\frac{X(\omega) \otimes Y(\omega)}{j\omega}, \quad (2)$$

where  $X(\omega)$  and  $Y(\omega)$  are the Fourier transformations of the input signals, and  $\otimes$  denotes convolution.

A two-tone model has been developed in this work. When the RF and LO ports are both driven by single-tone drivers with frequencies of  $\omega_1/2\pi$  and  $\omega_2/2\pi$ , respectively, the output of an ideal correlator can be described by the following equation:

$$k \int \cos(\omega_1 t + \varphi_1) \cos(\omega_2 t + \varphi_2) dt = \frac{k}{2} \left[ \frac{\sin(\omega_{\text{sum}} t + \varphi_{\text{sum}})}{\omega_{\text{sum}}} + \frac{\sin(\omega_{\text{diff}} t + \varphi_{\text{diff}})}{\omega_{\text{diff}}} \right] + c, \quad (3)$$

where

$$\begin{aligned} \omega_{\text{sum}} &= \omega_1 + \omega_2, \\ \omega_{\text{diff}} &= \omega_1 - \omega_2, \\ \varphi_{\text{sum}} &= \varphi_1 + \varphi_2, \\ \varphi_{\text{diff}} &= \varphi_1 - \varphi_2, \end{aligned} \quad (4)$$

and where  $k$  and  $c$  are both constants.

The output of an ideal correlator can therefore be thought of as containing two tones, namely, a summary-frequency tone (ST)  $\omega_{\text{sum}}$  and a differential-frequency tone (DT)  $\omega_{\text{diff}}$ . In the above equation, the ratio of the first term (ST) to the second term (DT) is  $\omega_{\text{diff}}/\omega_{\text{sum}}$ . Figure 4 shows the simulated differential-voltage spectrum gain of a periodic steady-state analysis, using 5 GHz and 4 GHz for the RF and LO frequencies, respectively. It can be seen in this figure that the DT gain is 0.35 dB and the ST gain is  $-19.4$  dB. The harmonics that interfere most with the output are DC and LO harmonics. From this simulation we can obtain the harmonic distortions as

$$\begin{aligned} \text{HD0} &= \text{Amplitude of DC/fundamental} = -51.4 \text{ dBc}, \\ \text{HD4} &= \text{Amplitude of LO/fundamental} = -31.8 \text{ dBc}, \end{aligned}$$

where in this case, the fundamental is the DT, and the amplitudes of LO and RF are 50 mV and 20 mV, respectively.

As a performance measure of the correlator, we borrow the conversion gain usually used for a mixer. The ST gain versus LO frequency, with LO frequency swept from 3 GHz to 10 GHz, is shown in Figure 5. The IF frequency is the difference between the RF and the LO frequencies and is fixed at 1 GHz, which means that the RF frequency is swept from 4 GHz to 11 GHz. Because an integrator is a lowpass filter with a DC pole, the gain decreases with increasing frequency, as expected.

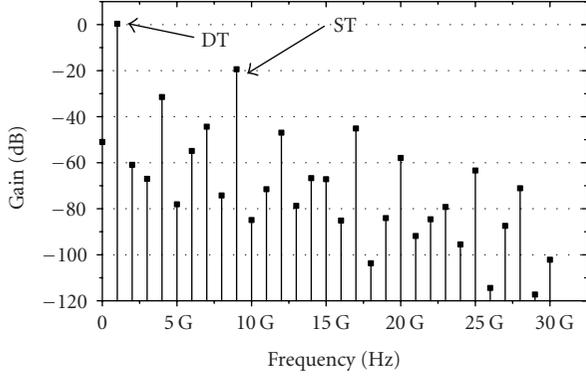


FIGURE 4: Output-spectrum gain (RF = 5 GHz, LO = 4 GHz).

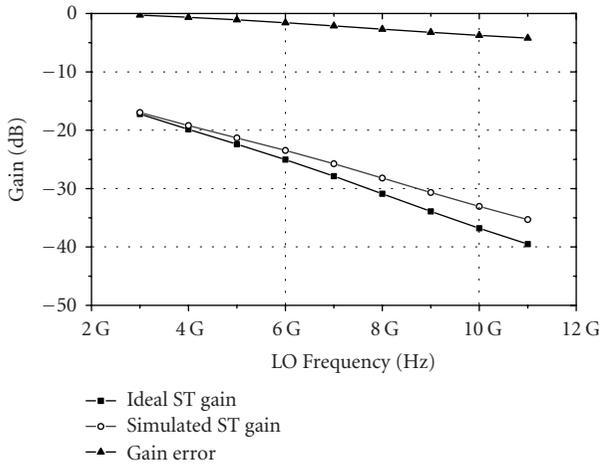


FIGURE 5: Comparison of the simulated and the ideal ST gain (RF = LO = 1 GHz).

Values of the output capacitances, including  $C_o$ , the gate-drain capacitance of  $M_1$ – $M_2$  and the gate capacitance of  $M_5$ – $M_6$ , will change as the output frequency increases, which will affect the ST behavior. To measure the high-frequency performance of the correlator, the output ST gain is compared with the ideal curve generated from the DT by adding  $20 \log(\omega_{\text{diff}}/\omega_{\text{sum}})$  to the DT gain (in dB). The quality factor of the capacitor decreases at high frequency, that is, becomes less capacitive, thus the simulated ST decreases less than the ideal value. Although the error between the two curves also increases with increasing frequency, as shown in Figure 5, this problem is not serious because  $\omega_{\text{sum}}$  also increases, which results in a reduction of the error at high frequencies. The following expression is used to calculate the normalized ST gain error:

$$\varepsilon = \frac{|G_{\text{ST}} - G'_{\text{ST}}|}{G'_{\text{ST}}} = |10^{E(\omega_{\text{sum}})/20} - 1| \frac{\omega_{\text{diff}}}{\omega_{\text{sum}}}, \quad (5)$$

where  $G_{\text{ST}}$  is the simulated ST gain,  $G'_{\text{ST}}$  is the ideal gain, and  $E(\omega_{\text{sum}})$  is the unnormalized ST gain error in dB.

Figure 6 shows the normalized ST gain error versus LO frequency. The normalized gain error does not change much

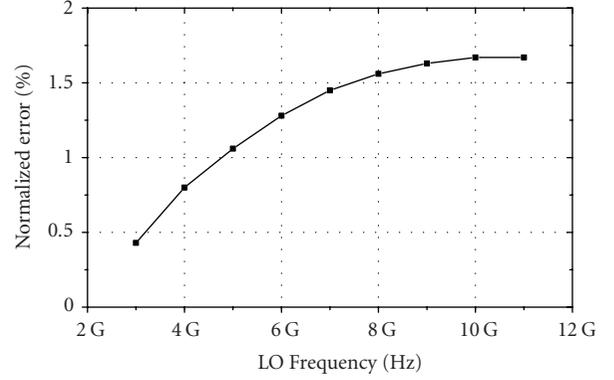


FIGURE 6: Normalized ST gain error (RF = LO = 1 GHz).

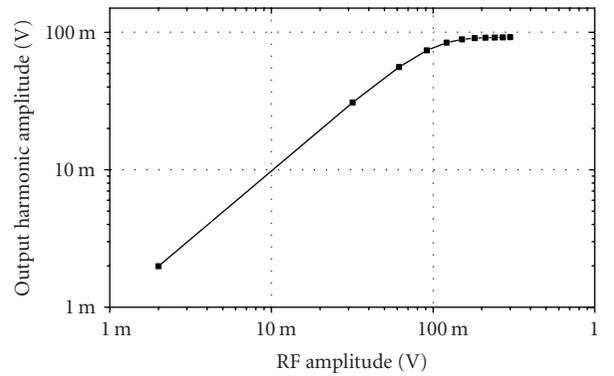


FIGURE 7: Output amplitude of DT versus RF amplitude (RF = 5 GHz, LO = 4 GHz).

with increasing frequency, and its value remains below 2% during the bandwidth region-of-interest.

The amplitude of the output DT versus the input RF signal is shown in Figure 7. The simulation shows that the conversion gain will saturate at approximately 150 mV of RF amplitude, which defines the maximum input value for the application of this circuit.

When the spectrum of the UWB signal is sampled with a 1 GHz frequency spacing, that is, the pulse signal is repeated every 1 nanosecond in the time domain, the spectra of the input signals are

$$\begin{aligned} X(\omega) &= x(-\omega) + x^*(\omega), \\ Y(\omega) &= y(-\omega) + y^*(\omega), \end{aligned} \quad (6)$$

where

$$\begin{aligned} x(\omega) &= \sum_{i=0}^N x_i \delta(\omega - i\omega_0), \\ y(\omega) &= \sum_{i=0}^M y_i \delta(\omega - i\omega_0), \end{aligned} \quad (7)$$

$\omega_0$  is the frequency spacing,  $N$  and  $M$  are the harmonic numbers, and  $x_i$  and  $y_i$  are the sampled values.

TABLE 1: Maximal normalized ST gain error.

IF (GHz)	1	2	3	4	5	6	7
$\epsilon_{\max}$ (%)	1.73	2.92	6.13	8.43	14.3	13.8	17.5

We can write the convolution of these two spectra as

$$X(\omega) \otimes Y(\omega) = \sum_{i,j}^{N,M} \begin{cases} x_i y_j \delta(\omega + i\omega_0 + j\omega_0) & (1), \\ x_i y_j^* \delta(\omega + i\omega_0 - j\omega_0) & (2), \\ x_i^* y_j \delta(\omega - i\omega_0 + j\omega_0) & (3), \\ x_i^* y_j^* \delta(\omega - i\omega_0 - j\omega_0) & (4), \end{cases} \quad (8)$$

where (1) and (4) are STs while (2) and (3) are DTs. In the two-tone frequency-swept simulation, the difference between the LO and RF frequencies is fixed at  $\omega_0$ , therefore the correlator output spectrum at  $\omega_0$  is the weighted sum of all DT simulation results. The high-frequency distortion of the output at  $k\omega_0$ , composed of STs, can also be approximately estimated by

$$\frac{1}{P} \sum_{s=k} \gamma_{x_{d,s}} \gamma_{y_{d,s}} \epsilon_{d,s} \quad (9)$$

where  $\epsilon_{d,s}$  is the normalized ST gain error described before, for summary and differential frequencies of the two input signals of  $s\omega_0$  and  $d\omega_0$ , and where  $s$ ,  $d$ , and  $k$  are all positive integers. The two coefficients  $\gamma_{x_{d,s}}$  and  $\gamma_{y_{d,s}}$  are the amplitude ratios of the actual input spectrum (that contributes to the specified ST (i.e.,  $k\omega_0$ ) in the two-tone model) to the corresponding spectrum in the simulation.  $P$  is the number of possible combinations of any two tones. Table 1 gives the maximal normalized error for several different two-tone simulations.

The noise performance defines the minimum limit of the input signals that can be processed by the circuit. The simulated single side-band (SSB) noise figure (NF) of the correlator is 16 dB at 1 MHz, for a LO frequency of 4 GHz. The major contributor to the noise is the active load. Device sizing to reduce noise is limited by the effects of loss in bias-voltage headroom and output dynamic range.

### 3.2. Transient simulation

In this section, we focus on the time-domain performance of the correlator. A UWB system is immune to multipath fading because it uses narrow pulses and can resolve reflections. Many resolvable path lengths between a given transmitter and receiver exist, and can be used for communication. In UWB applications, the received signals may also be distorted by the wireless channel, both indoor and outdoor. The multipath problem and the distortion of received signals during transmission in a wireless environment can be solved by the following baseband processor. Consequently, in the front-end, only the magnitude and polarity of input signals need to be considered.

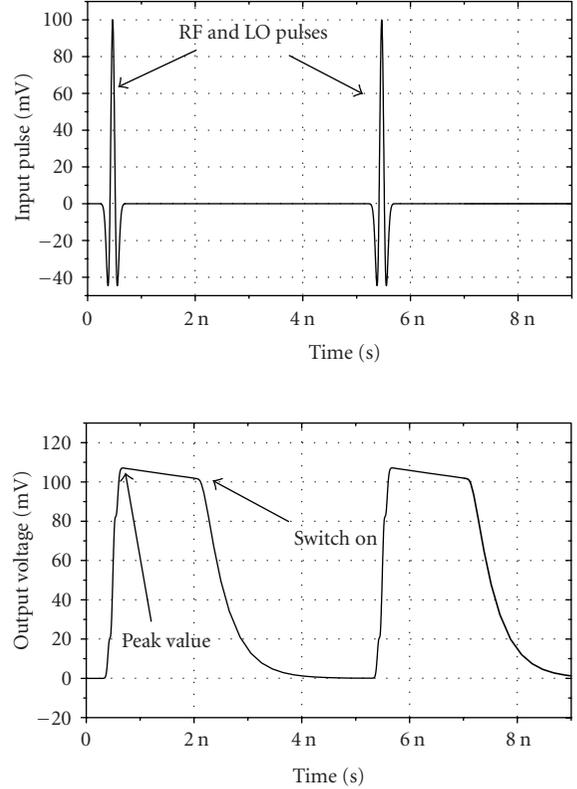


FIGURE 8: Transient simulation with RF and LO synchronized (the p-p voltage of both the RF and LO pulses is 160 mV;  $\tau_m = 177.2$  picoseconds and  $T = 5$  nanoseconds).

In the transient simulation, the impulse-signal shape is determined by [7]

$$s(t) = \left\{ 1 - 4\pi \left[ \frac{(t - nT)}{\tau_m} \right]^2 \right\} \exp \left\{ -2\pi \left[ \frac{(t - nT)}{\tau_m} \right]^2 \right\}, \quad (10)$$

where  $\tau_m = 177.2$  picoseconds and  $T = 5$  nanoseconds. The RF and LO pulses are time-shifted versions of  $s(t)$ , with a 144 mV p-p value for each. At the differential input port, the negative node is fixed to the bias voltage, and the pulse is added onto the positive net in the simulation. There are two possible kinds of application for the correlator. One requires integration of the output every pulse and detection of a single pulse, and the other requires integration for one symbol, including several pulses. The curves in Figures 8 and 9 show the simulation results of the above two kinds of applications, where the input pulses (RF and LO) are assumed to be exactly synchronized. As seen in Figure 8, after the cross voltage of the capacitor reaches its peak value of about 120 mV, the capacitor is shorted and discharged by the MOS switch and the output voltage then decreases to near zero. Figure 9 shows the result of ten pulses integrated together to form a ladder-like output; the peak voltage is about 300 mV.

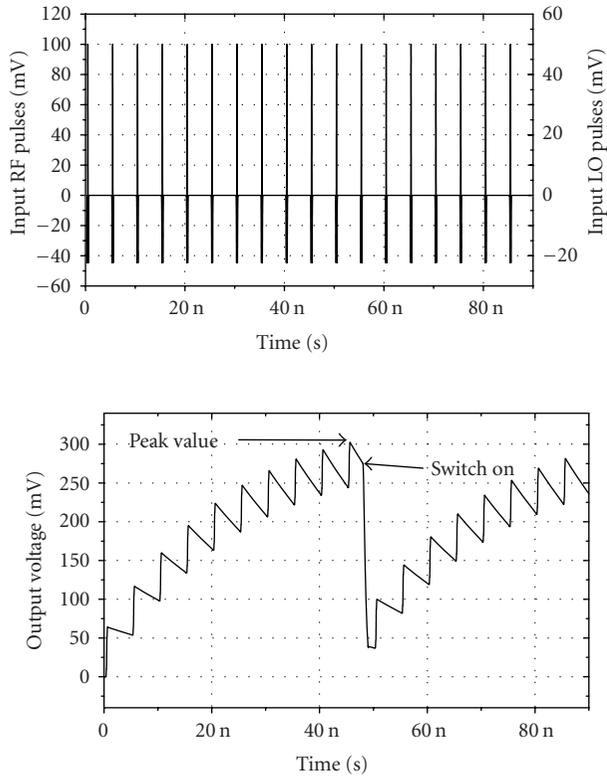


FIGURE 9: Transient simulation with RF and LO synchronized (the p-p voltages of the RF and LO pulses are 144 mV and 72 mV, respectively;  $\tau_m = 177.2$  picoseconds and  $T = 5$  nanoseconds).

The negative feedback composed of the active load and  $C_o$  will lead to a discharge of this capacitor, as illustrated by the output voltage dropping after integration of each pulse. This phenomenon becomes more obvious with increasing voltage across the load, as shown in Figure 9. For example, if a current flows from  $V_{o+}$  to  $V_{o-}$ , causing  $V_{o+}$  to increase, the drain-source voltage of  $M_1$  in Figure 3 will decrease and so will the drain current of  $M_1$ , which will then lower the capacitor charging current, or alternatively generate a negative discharging current on the capacitor after the integration. A cascode positive-channel metal-oxide semiconductor (PMOS) active load is used to increase its output resistance and to reduce the negative discharging current, though as a tradeoff, this results in an increase of the power supply voltage.

Figure 10 shows the output peak voltage versus the time that the centers of RF pulses are ahead of the LO pulses. It can be seen that the maximum of the peak voltage occurs at 20 picoseconds (i.e., when the LO pulses are 20 picoseconds earlier than RF pulses), which means that the latency of the predistortion module is about 20 picoseconds. This latency should be considered during signal acquisition and synchronization. The integration voltage on the capacitor load is sampled and the difference between the RF and LO pulses is evaluated based on the sampled value by the comparator.

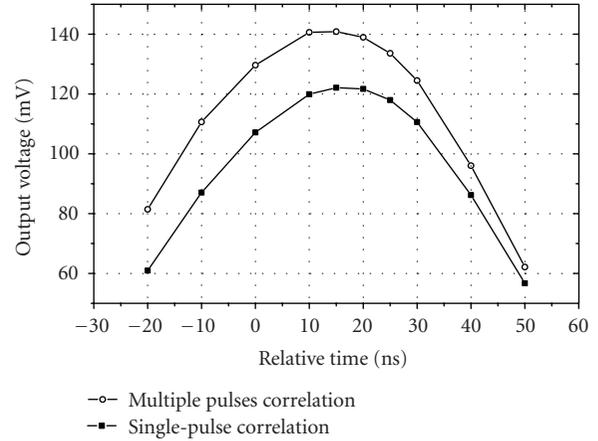


FIGURE 10: Peak voltage value versus the relative time (that the centers of RF pulses are ahead of LO).

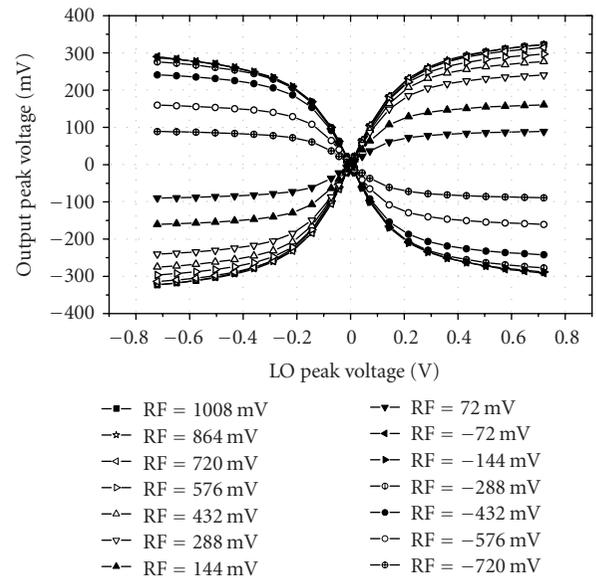


FIGURE 11: Output peak voltages versus LO magnitude and polarity.

Simulations of different pulse magnitude and polarity are shown in Figure 11 (all voltages in the figure are peak-to-peak values; single-pulse correlation case). As the input voltage increases, the output grows linearly until one of the two input signals begins to saturate. The response has a larger dynamic range for positive pulses than the negative pulses on the RF port because the collector current of  $Q_9$  or  $Q_{10}$  will decrease when a negative pulse exists on the base of these transistors; decreasing the gain of the GC.

#### 4. CONCLUSION

This paper has presented the design of a 3–10 GHz correlator for use in a UWB front-end. A standard GC is implemented with active current-source load, which can force the

output differential current to flow through a capacitor, leading to current integration on the capacitor. A novel technique for performance measurement of the correlator has been developed. The results of several simulations demonstrate that the new circuit design is practicable for impulse radio systems.

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