

# PN Sequence Preestimator Scheme for DS-SS Signal Acquisition Using Block Sequence Estimation

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*Received 10 February 2004; Revised 12 June 2004; Recommended for Publication by Xiang-Gen Xia*

An  $m$ -sequence (PN sequence) preestimator scheme for direct-sequence spread spectrum (DS-SS) signal acquisition by using block sequence estimation (BSE) is proposed and analyzed. The proposed scheme consists of an estimator and a verifier which work according to the PN sequence chip clock, and provides not only the enhanced chip estimates with a threshold decision logic and one-chip error correction among the first  $m$  received chips, but also the reliability check of the estimates with additional decision logic. The probabilities of the estimator and verifier operations are calculated. With these results, the detection, the false alarm, and the missing probabilities of the proposed scheme are derived. In addition, using a signal flow graph, the average acquisition time is calculated. The proposed scheme can be used as a preestimator and easily implemented by changing the internal signal path of a generally used digital matched filter (DMF) correlator or any other correlator that has a lot of sampling data memories for sampled PN sequence. The numerical results show rapid acquisition performance in a relatively good CNR.

**Keywords and phrases:** sequential estimation, PN sequence, acquisition, spread spectrum, digital matched filter.

## 1. INTRODUCTION

PN sequence acquisition is a precondition for stable and reliable spread spectrum communication. The research on PN sequence acquisition has been continuing for more than 20 years to improve its performance, stability, and acquisition speed [1, 2].

There are two representative methods for the acquisition of a PN sequence. One is a sequential estimation method that uses one of the important characteristics of the PN sequence generation with linear feedback shift register (LFSR) structure. That is, if  $m$  chips of the PN sequence can be estimated correctly from the received signal, these chips can be loaded into the  $m$ -shift-register generator to synchronize the system. In 1977, Ward and Yiu enhanced this method with recursive-aided sequential estimation [3]. In spite of its simple structure and rapid acquisition performance, this method cannot be used for low SNR radio environment because of the performance degradation and its instability. Several studies [4, 5, 6] have been done with a majority-

logic decoder to enhance the acquisition performance using a large number of parity-check sums for each chip. Recently, a seed-accumulating sequential estimation scheme [7] has been proposed by accumulating each chip of the received seeds of  $m$  chips, and another modified scheme [8] has been developed with a two-threshold decision logic which provides not only chip estimates but also the reliability of the chip estimates by finding  $m$  consecutive estimates.

The other is a serial-search method with a correlation circuit. In 1984, Polydoros and Weber clearly analyzed the performance of this method [9], especially with matched filter [10]. Although the matched filter method is known as very efficient and stable for PN sequence synchronization, it takes much more time than the sequential estimation method in a relatively good CNR environment because of its structural characteristics and sequence-search window uncertainty. Commercially, the matched filter is implemented with digital logic elements such as registers, adders, multipliers, and so forth [2]. Hence, a sampling rate for the PN sequence chip, bits per sample, and the correlating

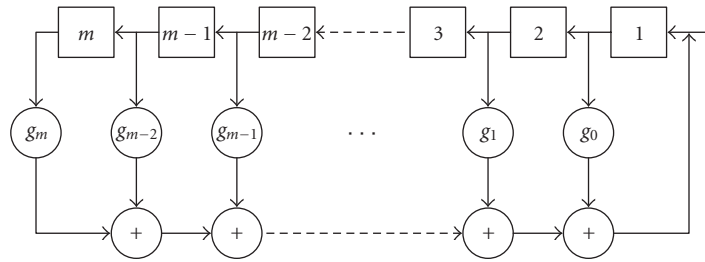


FIGURE 1: LFSR circuit for a generalized  $m$ -sequence generator.

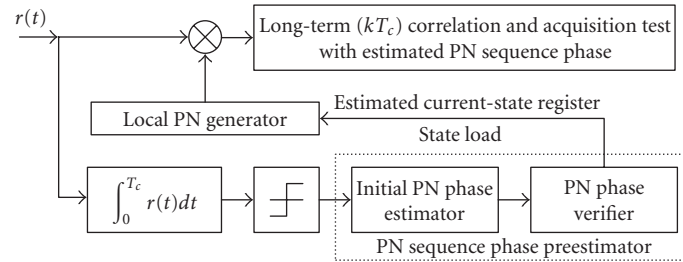


FIGURE 2: Acquisition model.

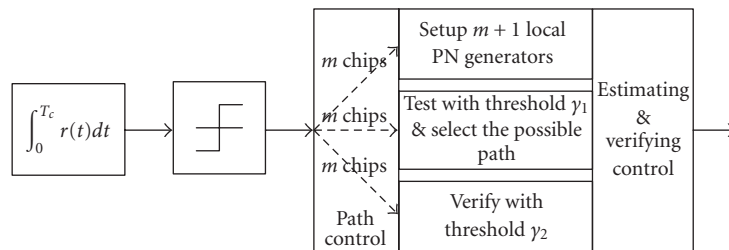


FIGURE 3: Detailed block diagram of the PN sequence phase preestimator.

(integration) period determine the structural complexity and acquisition performance of a digital matched filter (DMF) correlator.

Alternatively, we can adopt the adaptive detection scheme based on the MMSE (minimum mean-squared error) criterion to successfully deal with the multiple-access interference or multiuser detection, which requires an estimation process, training with known data sequence, or blind channel estimation [11, 12].

In this paper, we propose a preestimator scheme that can cooperate with a DMF correlator for PN sequence acquisition sharing the unused elements of the DMF structure within a given period of time (filling up the time of the DMF registers with the sampled PN chips or the given fixed operation time limits), and can analyze its performance. This scheme provides one-chip error correction capability of the initially loaded PN sequence chips on the LFSRs and a flexibility to manage structural resources of a correlator structure.

In Sections 2 and 3, the block sequence estimation (BSE) structure and its probabilistic performance are explained in detail, and the average acquisition time will be calculated in Section 4. Section 5 gives numerical results that show the

acquisition performance of the proposed scheme. Finally, we conclude our work in Section 6.

## 2. PN SEQUENCE BLOCK ESTIMATOR

PN sequence generator corresponding to a generator polynomial has an LFSR form illustrated in Figure 1. In this figure, the boxes represent the shift register where  $m$  is the number of the registers, circles containing subscripted letter coefficients  $g_m$  represent a connection if the coefficient is a 1 or no connection if the coefficient is a 0, and circles containing “+” mean modulo-2 adders or exclusive-OR gates [2]. The number of shift registers, connection coefficients, and modulo-2 adders depends on a given generator polynomial. This generator circuit is used for the local PN sequence generators of the proposed preestimator scheme. Because the explanation about this LFSR topic is beyond the scope of this paper, we will skip the details.

Figures 2 and 3 show a conceptual application diagram of the proposed scheme. This scheme consists of several components such as an integrator for chip duration  $T_c$ , a bit slicer, an estimator, and a verifier. As shown in Figure 2, if a correct

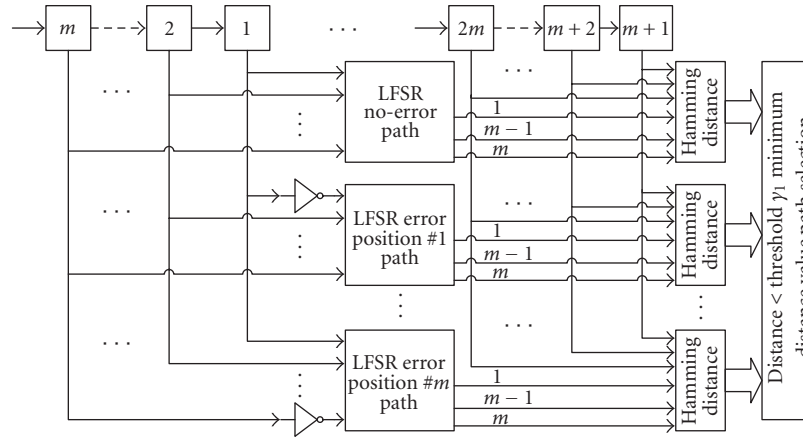


FIGURE 4: PN phase estimator.

PN sequence phase is estimated, this sequence can be loaded on a local PN generator and tested for a long time (given a period of time  $kT_c$ ), where  $k$  is a positive integer. In Figure 2, after finishing its operation with fail or success to estimate the correct PN sequence phase in a given operation time, the structure of the preestimator block will be disassembled and returned to the elements of the original correlator structure.

The proposed PN sequence phase preestimator works as follows.

- (1) Setup  $m+1$  local PN sequence generators (LFSR paths) with the first received  $m$  PN chips as follows:
  - (1) load  $m$  PN chips as the initial shift register values at a no-error LFSR path;
  - (2) load  $m$  PN chips as the initial shift register values inverting position #1 chip at the error position #1 LFSR path;
  - (3) load  $m$  PN chips as the initial shift register values inverting position #2 chip at the error position #2 LFSR path;
  - ⋮
  - ( $m+1$ ) load  $m$  PN chips as the initial shift register values inverting position # $m$  chip at the error position # $m$  LFSR path.
- (2) Receive the second  $m$  PN chips and shift all LFSRs by  $m$  times with a chip clock.
- (3) Test the Hamming distance between the second  $m$  PN chips and each register's residue values of the LFSRs.
- (4) Select an LFSR path having minimum distance.
- (5) If the selected path's minimum distance value is lower than threshold  $\gamma_1$ , go to (6).  
Else, go to (1) and repeat the previous steps because the estimating procedure failed.
- (6) Receive the third  $m$  PN chips and shift the selected LFSR path by  $m$  times with the chip clock.
- (7) Test the Hamming distance between the third  $m$  PN chips and the register's residue values of the survived LFSR path.
- (8) If the minimum distance is lower than threshold  $\gamma_2$ , go to (9).

Else, go to (1) and repeat the previous steps because the verifying procedure failed.

- (9) Optional test: long-term  $kT_c$  correlation and acquisition test with estimated PN sequence phase.

The above operation can be separated into two operators' work. One is the estimator (works from step (1) to step (5)) in Figure 4 that consists of  $m+1$  LFSR paths with one-error correction capability and chooses the best possible correct path. The other is the verifier (works from step (6) to step (8)) that confirms the survived path whether the selection is correct or not, as shown in Figure 5. The two operators' comparator circuit has a very simple structure with an LFSR. For providing one-error correction capability to the estimator,  $m+1$  local PN generator paths are needed as shown in Figure 4.

After receiving the first  $m$  PN chips, the no-error LFSR path stores these received  $m$  chips as the  $m$  register's initial values, and other  $m$  local LFSR path register values are transferred from the received buffers with one inverted chip that is corresponding to the chip error position buffer value to the path order of the local LFSR paths referred to in Figure 4. Among the  $m+1$  local LFSR paths, the one path that survived through the estimator test is assumed as a possible correct one. This test uses the Hamming distance comparison method between  $m$ -time-shifted local LFSR paths' register residue values and the second received  $m$  PN chip buffer values, path by path. After calculating the distances, we select one path that has the minimum distance value among the LFSR paths, and the selected path's Hamming distance is smaller than the given selection threshold  $\gamma_1$  to confirm whether the choice is correct or not. Hence, we can assume that the selected LFSR path is a possible correct path by the estimator.

The selected local LFSR path shifted by another  $m$  times with the chip clock will be compared with the third received  $m$  PN chips and tested with the verification threshold  $\gamma_2$  at the verifier in Figure 5. If the verification test passed, the proposed scheme declares success of the PN sequence acquisition and finishes its operation.

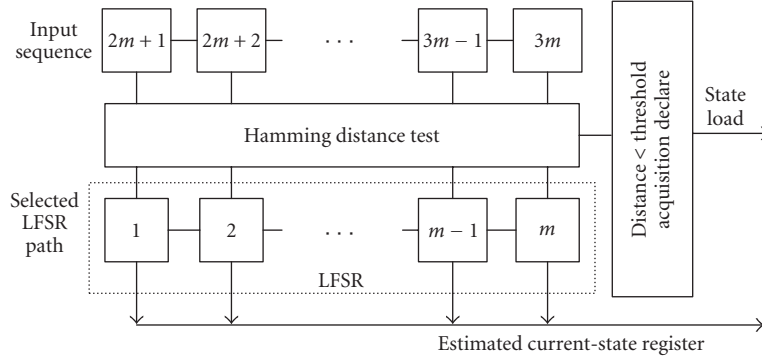


FIGURE 5: PN phase verifier for the verification mode.

TABLE 1: Number of registers.

Scheme		Number of registers
BSE		240
DMF correlator (128 chip)	2 samples/chip	2048
	4 samples/chip	4096
DMF correlator (256 chip)	2 samples/chip	4096
	4 samples/chip	8192

To make all LFSR paths uncorrelated with each other due to the relationship between each LFSR path's retained register values, the local LFSR path will be shifted more than  $m$  times with the chip clock. Therefore, the proposed scheme can finish all the estimation process in a minimum  $3m$  PN chip time at the best case, and it is the basis of rapid acquisition.

In the case where the proposed BSE scheme is used with the DMF correlator, Table 1 shows how many registers (bit memories) are required to implement the proposed scheme compared to a DMF correlator and gives an idea to share the furnished registers of a DMF correlator. We assume that the bits per PN chip sample are 8 and the length of the LFSR register  $m$  is 15.

### 3. DETECTION AND FALSE ALARM PROBABILITY

The probabilities of passing through the acquisition processes shown in Figure 6 are defined in Table 2. These probabilities can be calculated with combinational probability.

To calculate each probability in Table 2, we assume that the received chip error probability is  $P_e$  at the given CNR. The respective correct probability of the received PN chips to the incorrect path register values is  $1/2$ , and to the correct path registers value is  $1 - P_e$ . That is, when one correct LFSR path exists because there is none or one-chip error among the received  $m$  PN chips, the probability of the correct path selection will be calculate with  $P_e$ , whereas if a correct LFSR path does not exist or an incorrect LFSR path is selected, the following steps will use  $1/2$  instead of  $P_e$  because the values in the  $m$ -time shifted LFSR and the newly received  $m$  PN chips can be assumed as uncorrelated random sequences for each other.

As shown in Figure 2, the received PN chips have a hard-decision value "1" or "0" by the bit slicer. Hence, all probabilities can be calculated based on Bernoulli trial cases.

In the process of selecting one LFSR path among one correct and other  $m$  incorrect LFSR paths at the estimator, we can be faced up with selecting one of the  $m$  incorrect LFSRs. This is due to the fact that the received  $m$  PN chips having multiple errors and there is no prior information about the correct path. There are two cases for the force to choose an incorrect path with the probability  $P_{\text{PathMiss}}$ , in spite of one of the local LFSR paths being the correct path. First is when one of the incorrect paths always wins over the correct path in the comparison test to reach the second received  $m$  PN chips with the probability  $P_{\text{AF}}$  written as in (2). Multiple errors (more than the threshold  $\gamma_1$ ) in the received  $m$  PN chips to test the Hamming distance can lead the test to this result. Second is when more than one of the incorrect paths' Hamming distance testing results is equal to the correct path's. In this case, one of these paths will be selected arbitrarily and this choice can be incorrect with the probability  $P_{\text{EF}}$  expressed as in (3). Therefore,

$$P_{\text{PathMiss}} = P_{\text{AF}} + P_{\text{EF}}, \quad (1)$$

$$P_{\text{AF}} = \sum_{\gamma=1}^{\gamma_1} \left\{ 1 - \left[ \sum_{k=\gamma}^m \binom{m}{k} \left(\frac{1}{2}\right)^m \right]^m \right\} \cdot P(\gamma), \quad (2)$$

$$P_{\text{EF}} = \sum_{\gamma=1}^{\gamma_1} \sum_{k=1}^m \frac{k}{k+1} \binom{m}{k} \left[ \binom{m}{\gamma} \left(\frac{1}{2}\right)^m \right]^k \times \left[ \sum_{j=\gamma+1}^m \left[ \binom{m}{j} \left(\frac{1}{2}\right)^m \right] \right]^{m-k} \cdot P(\gamma), \quad (3)$$

where  $P(\gamma)$  is defined as follows:

$$P(\gamma) = \binom{m}{\gamma} P_e^\gamma (1 - P_e)^{m-\gamma}. \quad (4)$$

If a successful acquisition of the PN sequence with the detection probability  $P_D$  in (5) is declared, the receiver starts to disperse the received signal to recover the transmitted symbols or to operate a long-time verification circuit like a matched-filter correlator, if available, with the selected local

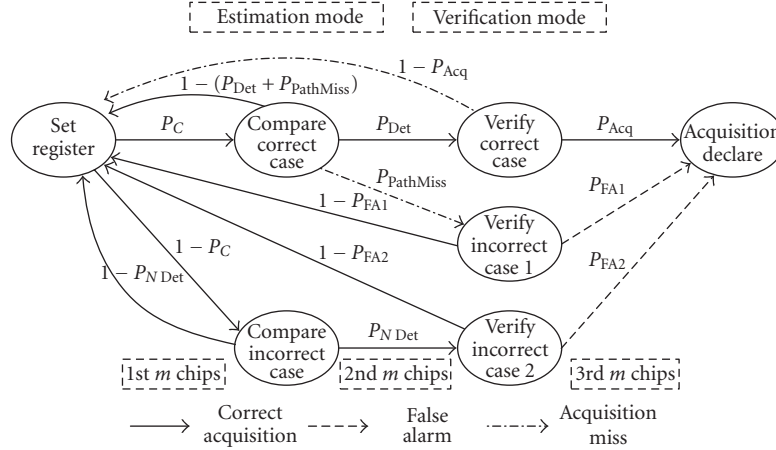


FIGURE 6: Acquisition process diagram.

TABLE 2: Probability definitions.

Probability	Definition
$P_C$	Probability of the one correct path existence among $m + 1$ LFSR paths
$P_{Det}$	Probability of the correct path selection among $m + 1$ LFSR paths
$P_{N Det}$	Probability of the one path selection among all incorrect LFSR paths
$P_{PathMiss}$	Probability of missing the correct path at the estimator
$P_{Acq}$	Probability of the acquisition declaration at the verifier
$P_{FA 1}$	Probability of the false acquisition declaration with $P_{PathMiss}$ at the verifier
$P_{FA 2}$	Probability of the false acquisition declaration with $P_{N Det}$ at the verifier

PN generator for a more reliable acquisition process:

$$P_D = P_C P_{Det} P_{Acq}, \quad (5)$$

where

$$P_C = \sum_{k=0}^1 \binom{m}{k} P_e^k (1 - P_e)^{m-k},$$

$$P_{Det} = \sum_{i=0}^{y_1} \binom{m}{i} P_e^i (1 - P_e)^{m-i} - P_{PathMiss}, \quad (6)$$

$$P_{Acq} = \sum_{k=0}^{y_2} \binom{m}{k} P_e^k (1 - P_e)^{m-k}.$$

However, even though the acquisition is declared, if the procedure is passed through the “verify incorrect case” node in Figure 6, it results in a false alarm with probability  $P_{FA}$  given by

$$P_{FA} = P_C P_{PathMiss} P_{FA 1} + (1 - P_C) P_{N Det} P_{FA 2}, \quad (7)$$

where

$$P_{FA 1} = \sum_{k=0}^{y_2} \binom{m}{m-k} \left(\frac{1}{2}\right)^m,$$

$$P_{N Det} = \sum_{k=0}^{y_1} \binom{m}{m-k} \left(\frac{1}{2}\right)^m, \quad (8)$$

$$P_{FA 2} = \sum_{k=0}^{y_2} \binom{m}{m-k} \left(\frac{1}{2}\right)^m.$$

Contrary to the false alarm case, there are two missing correct LFSR path cases. First is  $P_{PathMiss}$  from the estimator, and second is  $1 - P_{Acq}$  from the verifier. Hence, we can calculate the missing probability as follows:

$$P_{Miss} = P_C P_{PathMiss} + P_C P_{Det} (1 - P_{Acq}). \quad (9)$$

#### 4. AVERAGE ACQUISITION TIME

The signal flow graph of the PN code acquisition scheme is shown in Figure 7. After the acquisition declaration, normally to verify whether the acquisition declaration is correct or not, a long-time verification device, such as a matched filter correlator, should be adopted. To analyze the performance of the proposed acquisition scheme, if the scheme is declared as a correct acquisition, then the verification device will detect the PN sequence successfully.

The transfer function can be calculated with time delay  $Z$  as follows:

$$F(Z) = \frac{P_C P_{Det} P_{Acq} Z^2}{1 - R(Z)}, \quad (10)$$

where  $R_R(Z)$  represents the sum of signal flow transfer functions that have time delay because of the acquisition fail, and is computed from

$$R(Z) = R_{F1}(Z) + R_{C1}(Z) + R_{C2}(Z). \quad (11)$$

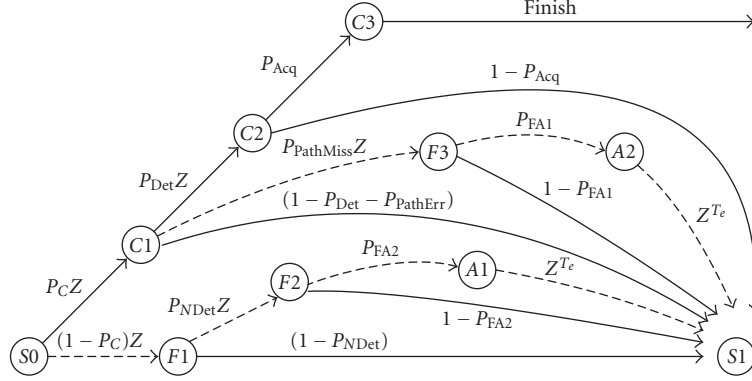


FIGURE 7: Signal flow graph.

In (11),  $R_{F1}(Z)$ ,  $R_{C1}(Z)$ , and  $R_{C2}(Z)$  are defined, respectively, by

$$\begin{aligned} R_{F1}(Z) &= (1 - P_C) \cdot [(1 - P_{NDet}) \cdot Z \\ &\quad + P_{NDet} \{ (1 - P_{FA2}) + P_{FA2} \cdot Z^{T_e} \} \cdot Z^2], \\ R_{C1}(Z) &= P_C \cdot [(1 - P_{Det} - P_{PathMiss}) \cdot Z \\ &\quad + P_{PathMiss} \cdot \{ (1 - P_{FA1}) + P_{FA1} \cdot Z^{T_e} \} \cdot Z^2], \\ R_{C2}(Z) &= P_C P_{Det} (1 - P_{Acq}) \cdot Z^2. \end{aligned} \quad (12)$$

The  $T_e$  is the penalty time to be wasted at the additional verification device, such as a matched filter correlator, because of the false alarm.

With this transfer function, the average acquisition time can be calculated by differentiating the transfer function and letting the time delay component  $Z = 1$ , resulting in

$$\begin{aligned} \overline{T_{Acq}} &= \frac{d}{dZ} [F(Z)]|_{Z=1} \cdot T_a \\ &= \left( \frac{2P_C P_{D11} P_{AC11}}{1 - R(1)} \right. \\ &\quad \left. + \frac{P_C P_{D11} P_{AC11}}{\{1 - R(1)\}^2} \cdot \frac{d}{dZ} [R(Z)]|_{Z=1} \right) \cdot T_a, \end{aligned} \quad (13)$$

where  $T_a$  is the  $m$ -chips receiving time, the examination time, filling up the registers of the LFSR with sampled chips and with  $m$ -time LFSRs shifted with the chip clock.

## 5. NUMERICAL RESULTS

In this paper, this chip error probability will be considered under an additive white Gaussian noise (AWGN) channel where its two-sided power spectral density is  $N_0/2$ . Also BPSK modulated signal with the  $P_e$  in (14) is assumed:

$$P_e = Q\left(\sqrt{\frac{2E_C}{N_0}}\right), \quad (14)$$

where  $E_C$  is the one-chip energy.

For the numerical calculations derived in the previous sections, the register length  $m$  of the LFSR PN sequence generator is 15. The penalty time  $T_e$  for the false alarm is assumed as  $128T_c$ .

In Figures 8 and 9, the detection and false alarm probabilities are plotted versus CNR with given  $\gamma_1, \gamma_2$ . Figure 8 shows that the detection probability plots continuously rise improving the acquisition performance until the saturation near 0 dB. In Figure 9, the false alarm probability nearly comes to be saturated at low CNR (worse than  $-5$  dB) because there can be multiple error chips among the received  $m$  PN chips to be loaded into the estimator's initial value, the acquisition and false alarm probabilities are small. In mid CNR (nearly from  $-5$  dB to  $-5$  dB), even though the estimator estimates the correct PN sequence phase, the false alarm probability can increase due to the erroneous received PN chips used for the Hamming distance test and the decision operation at the estimator and the verifier.

Figures 10 and 11 show the average acquisition time performances as a function of the given  $\gamma_1$  and  $\gamma_2$  parameters. Clearly, it is shown that the proposed structure can achieve rapid acquisition performance, especially when CNR is better than  $-5$  dB.

Figure 12 shows the comparison of the average acquisition time performance of the proposed BSE scheme in the case of  $\gamma_1 = \gamma_2 = 3$  with several other acquisition schemes: the recursion-aided sequential estimation (RASE) scheme [3] and the synchronization schemes using matched filter and fixed integration methods [2]. To calculate the average acquisition time of the matched filter and the fixed integration methods, we assume the best-probability case (lower-bound),  $P_D = 1$  and  $P_{FA} = 0$ . In addition, to be fair to the referenced schemes, the penalty time and the integration time are set the same as  $128T_c$ . From Figure 12, we can find that the BSE and the RASE show almost the same acquisition time performance when the CNR is higher than  $+4$  dB. Comparing the BSE to the remaining two schemes, which are assumed to be the best probabilistic cases, the proposed BSE shows faster acquisition time performance than the others in medium and high CNR.

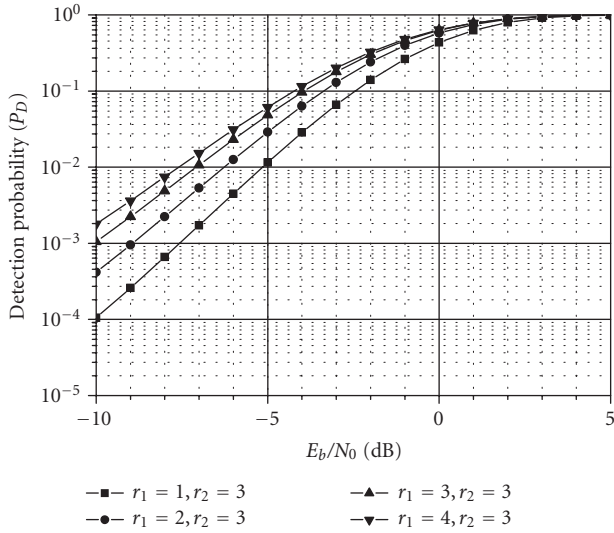


FIGURE 8: Detection probability  $P_D$  versus CNR, with given  $\gamma_2 = 3$  and  $\gamma_1$ .

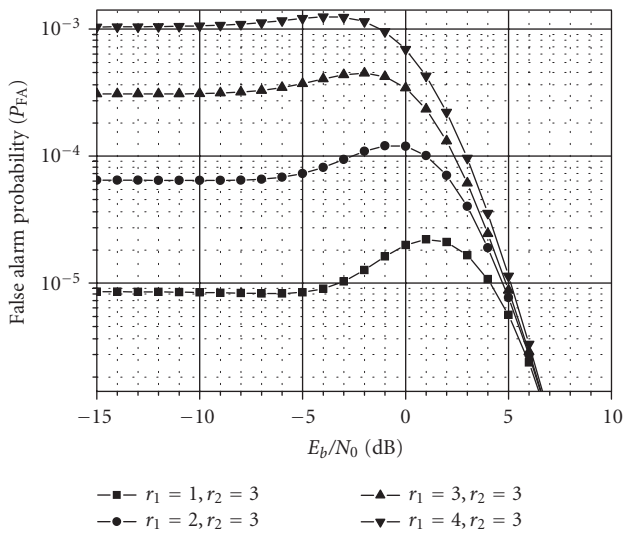


FIGURE 9: False alarm probability  $P_{FA}$  versus CNR, with given  $\gamma_2 = 3$  and  $\gamma_1$ .

**6. CONCLUSIONS**

In this paper, a PN sequence preestimator scheme using the BSE was proposed for the direct-sequence spread spectrum (DS-SS) system. The estimator, a part of the proposed BSE scheme, provides the enhanced chip estimates with threshold decision logic and one-chip error correction among the first  $m$  received chips. The one-error correction capability of the estimator is entitled by the  $m + 1$  local PN sequence generators. The verifier is used for the reliability check of the estimates with additional decision logic. From the numerical analysis, we observed that the average acquisition time is faster than the other referenced schemes in this paper. In special, the BSE scheme kept up fast acquisition time

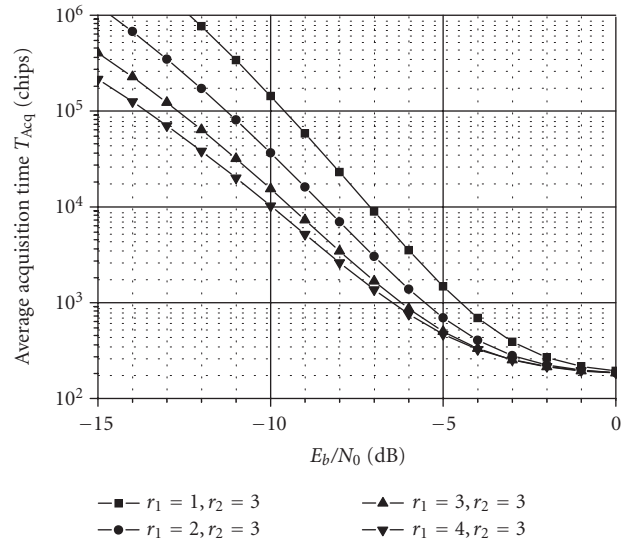


FIGURE 10: Average acquisition time  $\overline{T_{Acq}}$  versus CNR, with given fixed  $\gamma_2 = 3$  and  $\gamma_1$ .

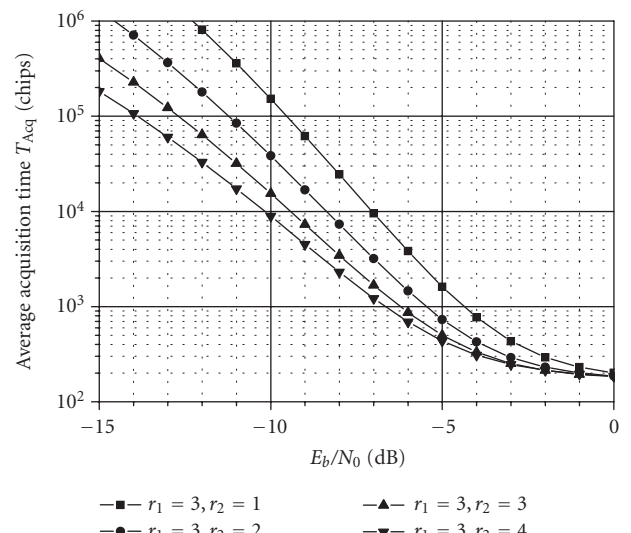


FIGURE 11: Average acquisition time  $\overline{T_{Acq}}$  versus CNR, with given fixed  $\gamma_1 = 3$  and  $\gamma_2$ .

until the CNR is fallen near to  $-4$  dB. The high hardware complexity of the proposed BSE scheme is affordable when the DMF correlator has already been used. That is, because the component parts of the proposed scheme are similar to those of the DMF correlator or any other correlator which has many memory elements, it can be easily implemented by changing the signal path connections and adding minimized glue logics.

Therefore, the proposed scheme can be used as an efficient rapid acquisition system or a flexible preestimator in advance of the other correlator operation depending on the quality of the received signal conditions to make up for the weak points of each other in mid-to-high CNR environment.

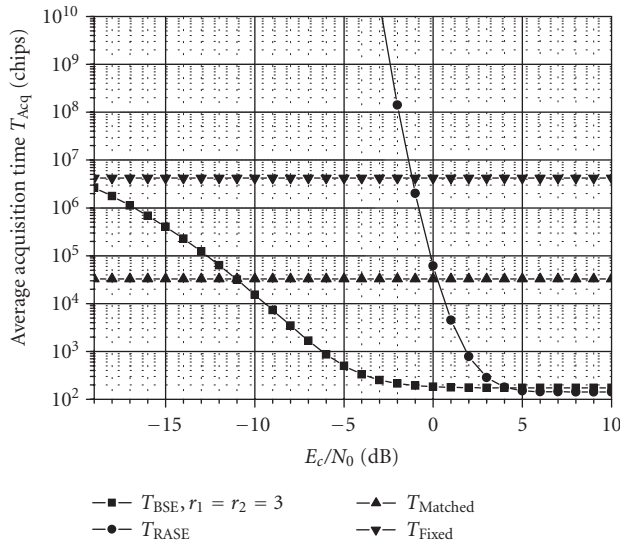


FIGURE 12: Comparison of average acquisition time with the proposed BSE, RASE, matched filter correlator, and fixed integration time case.

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