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Editorial

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With the increasing complexity of applications, rapid evolution of technology, and intense market competition in DSP consumer markets, the ability to quickly take a product concept to a working hardware/software demonstration is critical to the DSP industry. Key technologies required to meet this challenge include new types of programmable components that offer novel trade-offs between flexibility and efficiency, models for exchange of intellectual property, and computer aided design techniques for simulation, synthesis, verification, and integration of complex systems. The prototyping of modern DSP systems is especially complicated by increasing levels of application dynamics, and complex physical constraints. The papers in this special issue span a broad range of topics related to the rapid prototyping of DSP systems.

The first paper, by Tanougast et al., develops an approach for dynamic reconfiguration of FPGA implementations. The authors apply a temporal partitioning approach to the application dataflow graph with the objective of minimizing the FPGA resources required to meet a given performance constraint. Significant improvements in efficiency are demonstrated on a number of image processing applications.

The next paper, by Kuusilinna et al., describes the design of a large-scale emulation engine and an application example from the field of low-power wireless devices. The primary goal of the emulator is to support design space exploration of real-time algorithms. The emulator is customized for dataflow dominant architectures especially focusing on telecommunication related applications. The paper proves that real-time emulation of a low-power TDMA receiver is feasible at a clock speed of 25 MHz.

The third paper, by Oh and Ha, presents a software synthesis technique for minimizing buffer memory requirements of multimedia applications. This technique starts with a given schedule of the application dataflow graph, and is based on decomposing buffering requirements into global buffers and local pointers into these buffers. Methods for sharing global buffers and efficiently managing the local pointer buffers are developed in this framework. Large reductions in memory requirements are reported when applying these techniques to a JPEG encoder and an H.263 encoder.

The next paper, by Zhang and Parhi, focuses on an FPGA implementation of a (3,6)-regular low-density parity-check code (LDPC) decoder. In the past few years, the recently rediscovered LDPC codes have received a lot of attention and have been widely considered as next-generation error-correcting codes for telecommunication and magnetic storage. Unfortunately, the direct fully parallel decoder implementation usually incurs too high hardware complexity for many real applications. Hence, partly parallel decoder design approaches that can achieve appropriate trade-offs between hardware complexity and decoding throughput are highly desirable. Applying a joint code and decoder design methodology, this paper develops a high-speed (3,6)-regular LDPC code partly parallel decoder architecture. This implementation supports a maximum symbol throughput of 54 Mbps and achieves a BER of 10^{-6} at 2 dB.

In the paper by Fox and Turner, FPGA is used as rapid development platform for DCT approximations. The approximations are used to control the coding gain, MSE,

quantization noise, hardware cost, and power consumption by optimizing the coefficient values and the datapath world lengths. Lagrangian local search method is used to optimize the coefficients for the desired controlled parameters. Xilinix FPGA is used to rapidly prototype the DCT architecture with near optimal coding gain. The developed design methodology allows trade-offs among coding gain, hardware cost, and power consumption.

The next paper, by Carreira et al., describes an approach for FPGA-based design of FIR filters using the method of peak-constrained least squares for controlling the frequency response. The approach allows one to trade off passband-to-stopband energy ratio with FPGA resource requirements without altering the minimum stopband attenuation. Implementation of the approach utilizes JBits, which is a Java interface for controlling the configuration bitstream of Xilinx FPGAs.

In the next paper, by Spivey et al., a framework for rapid prototyping FPGA-based systems is presented. The framework "logic foundry" targets the integration of various DSP architecture design levels (or modules) and components. Four areas of integration: design flow integration, component integration, platform integration, and software integration are presented. Experimental results on Xilinix FPGA of an incrementer design and turbo decoder design show the use of the logic foundry for rapid prototyping. The framework is very flexible; it can be used as an integrated design environment or different modules can be used as stand-alone tools that can be integrated with other environments.

The paper by Madahar et al. presents case studies of adaptive beamformer applications for radar and sonar using a design environment and rapid prototyping methodology developed under the ESPADON (Environment for Signal Processing and Rapid Prototyping) project. ESPADON builds on existing tools, including Ptolemy Classic, GEDAE, and Handel-C, to provide an integrated process for reducing the cost and development time involved in implementing military signal processing applications. The paper focuses on demonstrating the productivity gains achieved through the ESPADON approach.

The next paper, by Bednara et al., develops a design method for mapping digital linear controllers with large signal processing requirements into efficient FPGA implementations. A case study of an inverse pendulum controller is used to illustrate the ideas and demonstrate the advantages of the proposed design techniques compared to software implementation.

The last paper, by Jones and Cavallaro, addresses one of the main challenges in developing design methodology for rapid prototyping which is the transition from simulation to a working prototype of a system. The developed design methodology is based on using an appropriate design language to bridge the gap between simulation and prototyping. Such an approach combines the strengths of simulation and prototyping, allowing the designer to develop and evaluate the target system partly in simulation on a host computer and partly as a prototype on embedded hardware. Several software tools have been developed for implementing the proposed design methodology. It has been successfully used in the development of a next-generation code division multiple access (CDMA) cellular wireless communication system.

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