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Design and Implementation of MC-CDMA Systems for Future Wireless Networks

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The emerging need for high data rate wireless services has raised considerable interest in MC-CDMA systems. In this work, we describe an MC-CDMA system design process for indoor propagation scenarios. The system specifications and simulations are firstly given, and then implementation aspects on a mixed, multi-DSP and FPGA architecture are presented. In order to reduce development cycle, we propose the use of efficient design methodologies to improve development steps such as complexity evaluation, system distribution according to the architecture, and hardware-software code generation. Implementation results of the considered MC-CDMA system are then given.

Keywords and phrases: MC-CDMA, multi-DSP-FPGA architecture, codesign methodology, hardware-software distribution.

1. INTRODUCTION

The European third-generation (3G) terrestrial mobile system under deployment aims at offering a large variety of circuit and packet services and greater capacity compared to second-generation (2G) systems. The evolution from 2G to 3G corresponds to adapting a new air interface but most of all to a change of focus from voice to multimedia. Fourth generation (4G), as for it, will be defined by the ability to integrate heterogeneous networks, especially radio mobile networks and wireless local area networks (WLAN), that is, to offer access to all services, all the time and everywhere [1]. Besides, the rapid growth of Internet services and the increasing interest in portable computing devices are likely to create a strong demand for high-speed wireless data services. Presumably, it is anticipated that systems with a maximum information bit rate of more than 2–20 Mbps in a vehicular environment and possibly 50–100 Mbps in indoor to pedestrian environments will be needed, using a 50–100 MHz bandwidth. Key issues to fully meet these evolution perspectives are based upon the most efficient use of scarce spectrum resources, and upon the advent of reconfigurable radio conceivable due to the emergence of software defined radio (SDR) equipments [2].

On the one hand, the multicarrier code-division multiple-access (MC-CDMA) modulation scheme has already proven to be a strong candidate as an access technique for broadband cellular systems [3]. Different concepts based on the combination of multicarrier (MC) modulation with direct-sequence CDMA (DS-CDMA) have been introduced in 1993 [4, 5, 6, 7]. Since that time, owing to its high spectral efficiency and high flexibility, MC-CDMA scheme has become a promising access technique for 4G air interface. MC-CDMA benefits are for example highlighted in [8]; it is demonstrated that, with respect to universal mobile telecommunications system (UMTS) and International Mobile Telecommunications 2000 (IMT2000) requirements based on a 5 MHz bandwidth channel, a net bit rate up to 4 Mbps with a 1/2 rate channel code and even 6 Mbps with a 3/4 rate code could be assigned to a single user for indoor but also macrocellular environments with a vehicular

mobility. Thus, MC-CDMA is nowadays considered as a very promising technique, specifically for the downlink of the future cellular mobile radio systems. Then, MC-CDMA is for example studied within the European IST project MATRICE (MC-CDMA transmission techniques for integrated broadband cellular Systems)[1]. This work has been partly carried out within this project MATRICE which aims at defining a new air interface for 4G systems.

On the other hand, the advent of such wireless communication systems also depends on the use of optimized embedded architectures and consequently of advanced design methods. Due to increased complexity applications, achieving high performances solutions is no more guaranteed by fully software (SW) implementation, using general-purpose processors (GPP) or digital signal processors (DSP), or fully hardware (HW) implementation on application specific integrated circuits (ASIC). Thus, heterogeneous architectures based on the combined use of reconfigurable HW components as field programmable gate array (FPGA) and reprogrammable SW processors such as DSP represent attractive and appropriate solutions for complex radiocommunication systems implementation and rapid prototyping. As a result, concurrent design, or codesign, methods become convenient to favour reduced development cycle for SDR system design [9]. These methods notably make possible efficient design spaces exploration to achieve an optimized matching between developed algorithms and targeted architectures [10].

In this context, an implementation of an airport data link based on MC communications was proposed in [11]. Besides, special focus on equalisation receiver design [12] or system consumption [13] can also be found. In a general way, this work aims at investigating MC-CDMA system design in the 4G context, from system definition to implementation under real-time constraints. This paper is dedicated to the study of MC-CDMA for indoor propagation scenarios. This first step is necessary to guarantee the feasibility of the implementation under real-time constraints. According to channel properties, different configurations for a MC-CDMA downlink air interface are proposed and simulated.

Implementation results on a heterogeneous platform combining DSP and FPGA are also presented. Our implementation approach is based on specific codesign methods in order to propose an efficient design flow integrating system modelisation, algorithms complexity evaluation, architectural exploration, automatic code generation, and implementation on the testbed platform.

This paper is organized as follows. In Section 2, first of all, the main features of the studied MC-CDMA system are presented. Furthermore, used heterogeneous platform is described, and the benefits of our codesign approach will be highlighted. In Section 3, system parameters are presented and simulation results are given. Section 4 deals with complexity analysis of studied MC-CDMA functions, whereas Section 5 presents implementation aspects of our codesign approach on the mixed architecture. Finally, Section 6 summarizes the results and conclusions are given.

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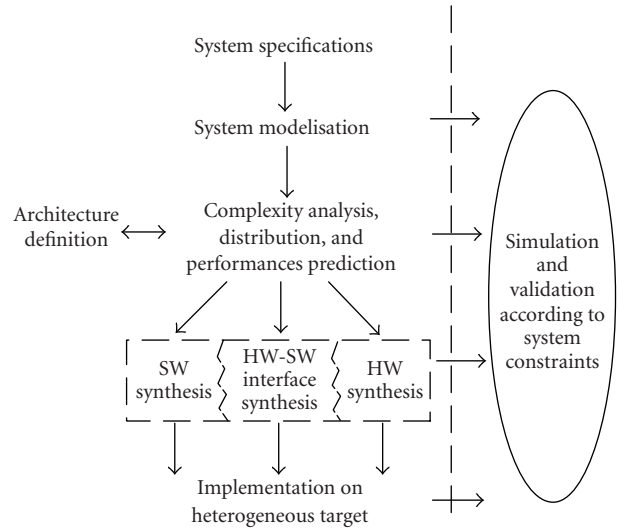

Figure 1: Generic codesign flow.

2. MC-CDMA SYSTEM DESIGN

codesign flow enables a top-down design from a system modelisation step to implementation on a prototyping board under real-time constraints, as illustrated in Figure 1. The first step aims at establishing MC-CDMA system specifications according to channel properties. Once validated, the system modelisation will then be used as an entry point in the architectural design. This important step deals with HW-SW distribution according to the specified functions complexity and the available architecture. Accurate modelisation is required to efficiently investigate various implementation solutions according to real-time constraints, such as throughput and consumption. Then, automatic synthesis of the adopted solution, both for the SW part, the HW part, and the interfaces, leads to a reduced development time and reliable solution.

2.1. MC-CDMA system modelisation

The MC-CDMA air interface allows high-capacity networks and robustness in the case of frequency-selective channels, taking benefits from CDMA capability offered by the spread spectrum technique, and MC modulation as orthogonal frequency division multiplex (OFDM). A possible generic downlink transmission scheme is depicted in Figure 2.

Each user data can be simultaneously processed at the spreading step before MC modulation. In the following, due to their good properties for the downlink [14], Walsh-Hadamard (WH) spreading sequences will be considered. The presented MC-CDMA configuration is based on the transmission of multiple data per MC-CDMA symbol for each user. Data $d_j^i(n)$ denotes the ith, $1 \le i \le N_b$, data transmitted by user j, $1 \le j \le N_u$, in the nth MC-CDMA symbol.

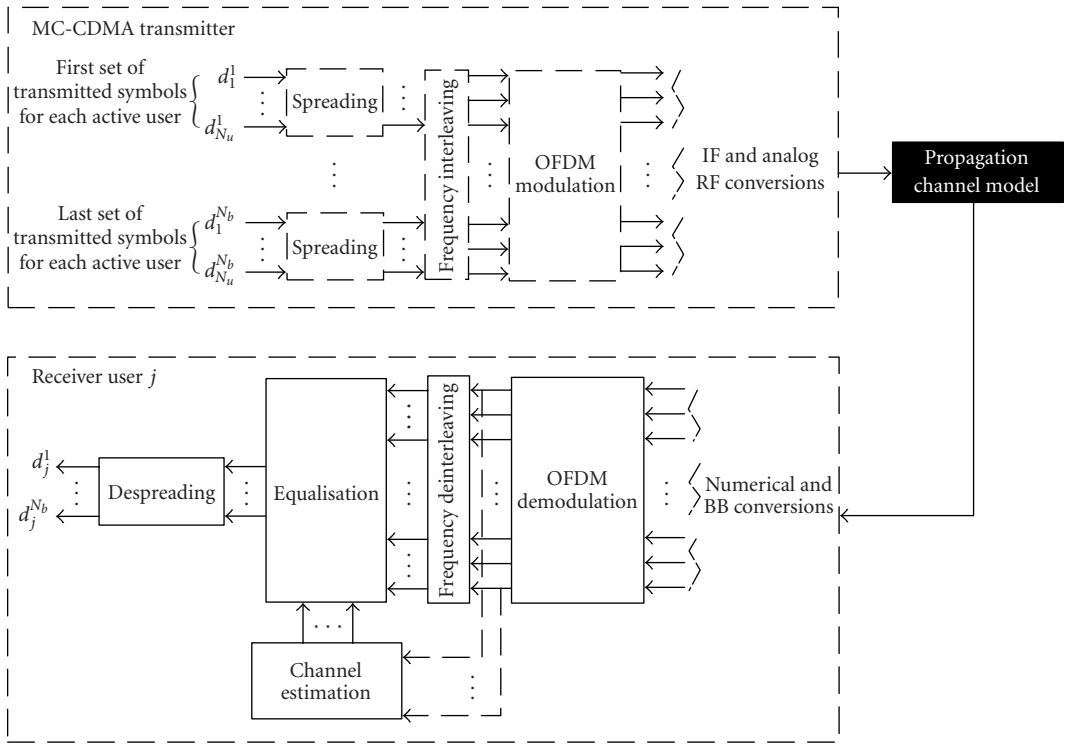

Figure 2: Studied MC-CDMA transmitter and receiver.

The maximum number of available users, which is also equal to the length of the WH spreading sequences, will be denoted N_u. The total number of subcarriers is $N_c = N_z + N_{cu}$, where N_z and N_{cu} are the number of unused and used subcarriers, respectively. Therefore, the number of data transmitted by each user in one MC-CDMA symbol is $N_b = N_{cu}/N_u$. Frequency interleaving is performed in order to fully exploit the frequency diversity offered by OFDM modulation.

At the receiver part, despreading is done according to the specific user sequence after equalisation in the frequency domain. The system synchronisation and intermediate frequency (IF) and baseband (BB) conversions problems are beyond the scope of this paper and will not be addressed. Among various equalisation techniques, we especially focus on single-user detection techniques. Channel estimation function can efficiently be performed by using pilot subcarriers insertion. The arrangement of these pilots must guarantee an optimum sampling of the channel transfer function in time and in frequency, depending on the bandwidth coherence and on the time coherence of the channel [15].

Obviously, MC-CDMA system offers high flexibility in resources (spectral efficiency, number of users) allocation which consequently induces large design spaces. As a result, high-level design methods are convenient in order to deal with such complexity and for efficient implementation.

2.2. Description of the proposed codesign approach

Most of radiocommunication systems designed on heterogeneous platforms are faced by the complexity of mixing SW and HW design flows. Functions distribution according to HW or SW mostly depends on designers experience. Besides, the matching between algorithm and architecture and estimation performances for multicomponent architecture is rarely addressed.

Thus, as illustrated in similar works [16, 17], a high-level specification is required to improve HW-SW distribution and combined simulation. Our purpose is to propose an efficient top-down design flow, making possible efficient architectural choices taking into account specified algorithms and heterogeneous target properties. Besides, in order to favour reusability and to reduce design process duration, a multisource integration, as well as HW description language (HDL) sources such as C codes, is required. As illustrated in Figure 3, our design process is based on the concurrent use of two codesign methods and their associated tools: the codesign methodology for embedded systems (CoMES) methodology [18], and the algorithm architecture adequation [19] (AAA) methodology; "Adequation" is a French word meaning an efficient matching. The first method is used for system modelisation and simulation, algorithms complexity evaluation, and architectural design, whereas the second one is used for functions distribution and code generation.

CoMES modelisation combines a graph model with C-coded algorithms, allowing complete system simulation without any assumption on architecture. Functions activity and complexity can then be evaluated using a profiling step. In a second part, the target architecture can be defined as a set of interconnected HW and SW processors. Finally, functions distribution on the multicomponent architecture can be studied according to system attributes such as time

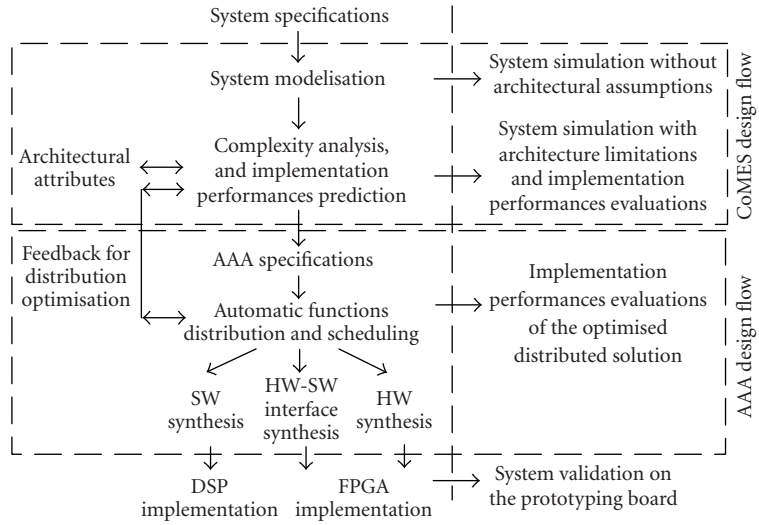

Figure 3: Considered design flow.

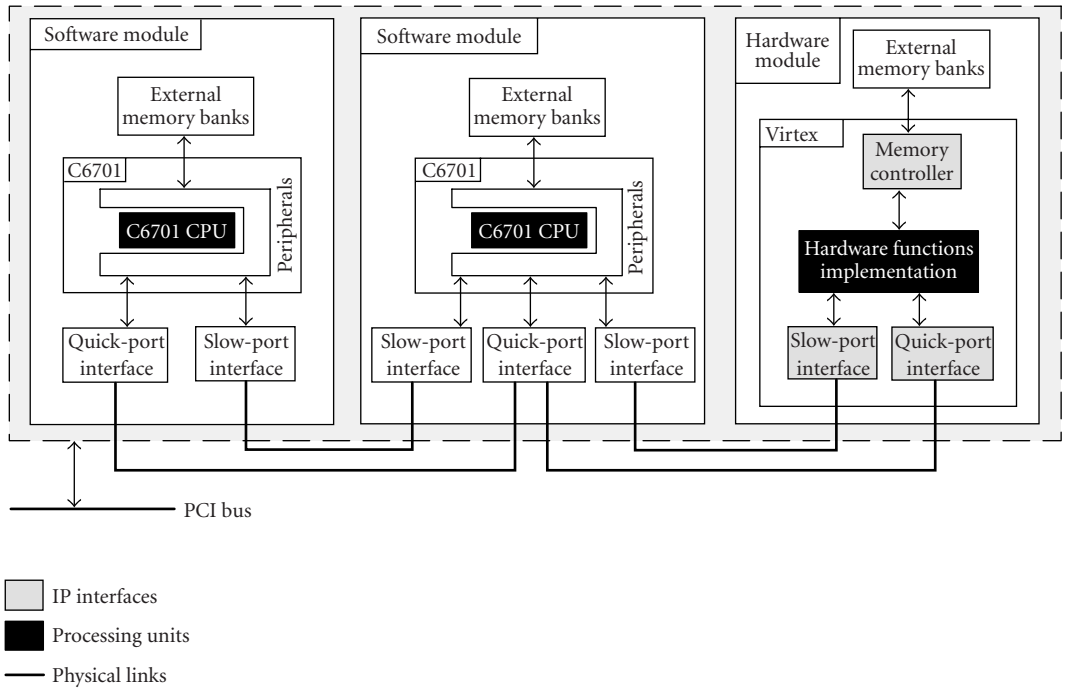

Figure 4: Heterogeneous architecture description.

execution on each component, data communication durations, and intercomponent interfaces behaviour. At this step, we can obtain a fully validated and detailed performances estimation of the mapped functions on the distributed architecture. The AAA methodology, as for it, is firstly used for functions automatic distribution, taking into account the different complexity parameters given by the previous step. This feedback makes possible accurate system evaluation. Once an efficient matching between functions and architecture has been found, the AAA methodology allows for algorithms and inter-component communications code generation, as well as for C generation and for VHDL generation.

The next part presents the used architecture for the MC-CDMA system implementation.

2.3. *Testbed architecture description*

Our prototyping platform is based on a peripheral component interconnect (PCI) Sundance Multiprocessor motherboard where two DSP-based modules and one FPGA module are plugged. As illustrated in Figure 4, two different communication formats are used: a 8-bit bidirectional format, denoted by slow port, allowing 20 Mbps transfer rate, and a 16-bit bidirectional format, denoted by quick port, allowing 200 Mbps throughput.

Table 1: Propagation channel parameters.

Parameters	Channel parameters
Maximum delay $\tau_{\max}$	390 ns
Delay spread σ_τ	50 ns
Measured 50% coherence bandwidth B_c	11 MHz
Measured 50% time coherence T_c	15 ms
Typical Doppler shift f_D at 1 m/s	17.33 Hz

Each SW module uses the TMS320C6701 DSP from Texas Instrument. This component is based on a very long instruction word (VLIW) architecture making it possible to compute 8 operations per cycle at a 167 MHz frequency. The FPGA is a XCV400 Virtex with 400 Kgates, corresponding to 2400 logic blocks. Memory blocks are also available in the FPGA. Dedicated components are used on the SW modules to make possible data exchanges between the DSP peripherals and the communication ports. Besides, HW intellectual property (IP) cores are provided to be inserted in the FPGA component to control the communication channels. The FPGA is configured using a bitstream sent by a DSP. The described codesign approach will be applied to this architecture for system implementation.

The next part presents MC-CDMA system parameters and simulation results according to the used channel model.

3. SYSTEM DEFINITION

For indoor propagation scenarios, we considered the BRAN-A channel as defined in [20], with a frequency carrier f_c = 5.2 GHz. In our simulations, the propagation channel will consist of 18 power loss paths with a flat Doppler spectrum on each path. In Table 1, the required channel parameters used to establish our simulation model for the propagation scenario are summed up.

This channel model has been implemented on the prototyping board presented in Section 2 in order to simulate the studied MC-CDMA system. The system parameters are chosen according to the time and frequency coherence of the channel in order to reduce intersubcarrier interferences (ICI) and intersymbol interferences (ISI). Besides, investigated MC-CDMA configurations are designed to propose high throughput and high capacity solutions for indoor scenarios. From the system model illustrated in Figure 2, the offered net bit rate per user can be expressed as follows:

$$D_u = \frac{nN_{cu}}{N_u(T_u + T_g)} = \frac{nN_{cu}}{N_u(N_c/F_s + T_g)} = \frac{nN_b}{(N_c/F_s + T_g)}, \quad (1)$$

where

(i) n is the bits number per symbol according to the used modulation. In the following, QPSK modulation will be considered ($n = 2$);

(ii) N_{cu} corresponds to the number of used subcarriers per MC-CDMA symbol;

(iii) $T_u + T_g$ is the whole MC-CDMA symbol duration, with a sampling frequency denoted by F_s. T_g is the guard interval duration. According to $\tau_{\max}$ value and in order to avoid ISI, T_g will be taken equal to 0.8 microseconds.

Table 2: Configurations parameters.

Parameters	Configuration I	Configuration II
Sampling frequency F_s	20 MHz	50 MHz
Number of total/used subcarriers (N_c/N_{cu})	64/48	256/192
Symbol/guard interval duration (T_u/T_g)	3.2 μs/0.8 μs	5.12 μs/0.8 μs
Subcarrier spacing (Δf)	321.5 kHz	195.3 kHz
Used bandwidth (W)	15.4 MHz	37.5 MHz
Number of users (N_u)—full-load system	4, 8, 16	16, 32, 64
Number of symbols per user (N_b)	12, 6, 3	12, 6, 3
Net bit rate per user (D_u)	6, 3, 1.5 Mbps	4, 2, 1 Mbps

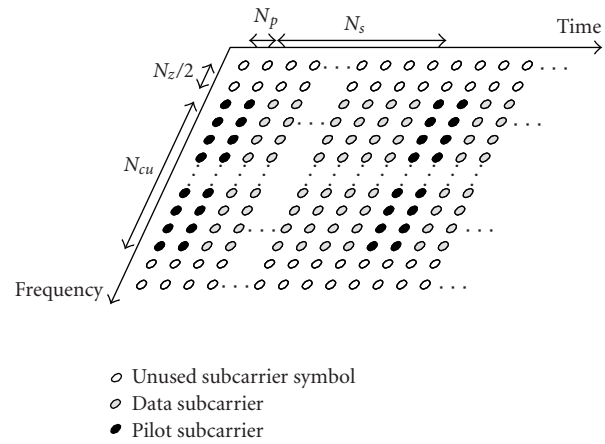

Figure 5: MC-CDMA frame structures.

The first proposed configuration, which parameters set is summed up in Table 2, is based on HIPERLAN Type 2 specifications with a 20 MHz sampling frequency. The ratios $O_g = T_u/(T_u + T_g) = 0.8$ show a low spectral efficiency loss due to guard interval insertion, which corresponds to a power efficiency loss equal to 0.97 dB.

In the second studied configuration, a 50 MHz sampling frequency is targeted to achieve a better tradeoff between bit rate and users capacity. In that case, $O_g = 0.86$ leads to a power efficiency loss equal to 0.63 dB. Besides, in both cases, Doppler shift is very low compared to the subcarrier spacing.

An appropriate approach for channel estimation in high-speed packet transmission is the use of a dedicated pilot symbol periodically inserted in the transmission frame. Furthermore, the very high ratio between the BRAN-A channel time coherence and the MC-CDMA symbol duration induces very slow channel evolution during the transmission of each symbol. Thus, the considered frame structure, illustrated in a general way in Figure 5, includes $N_p = 1$ pilot symbol at the beginning of each frame and N_s additional MC-CDMA data symbols per frame.

Table 3: Frame structure parameters.

Parameters	Configuration I	Configuration II
Number of data symbols per frame N_s	100/1000	100/500
Frame duration	400 μs/4 ms	592 μs/3 ms

Then, channel estimation is processed from the pilot symbol received at the beginning of each frame. As a result, nonideal channel estimation parameters impact on the quality of the transmission could be studied. Moreover, a constant power is allocated to pilots for all configurations. Simulations were performed considering a 1 m/s mobile speed. Table 3 gives the different simulated frame structures.

Besides, we investigated different detection techniques: maximum ratio combining (MRC), equal gain combining (EGC), orthogonality restoring combining (ORC), and suboptimal minimum mean square error (MMSE) techniques [21]. This last one is done using a fixed signal-to-noise parameter at 12 dB for the MMSE coefficients computation. Figure 6 illustrates the BER performance of considered single-user detectors for configuration I with $N_u = 8$, whereas Figure 7 represents performance for configuration II with $N_u = 32$, both in the full-load case.

The depicted curves obviously demonstrate efficiency of MMSE-based detector compared to others techniques. Besides, the two detectors using linear channel equalisation, that is, ORC and MMSE detectors, are more sensitive to inaccurate channel estimation than diversity combining detectors such as EGC.

According to the presented configurations and the frame structure, a tradeoff between the power allocated to pilot symbols and the performance degradation resulting from channel estimation errors should be found. A similar approach as described in [22] could be used.

In the following parts, we present the MC-CDMA system implementation results and the different steps of our design methodology used from system simulation to integration.

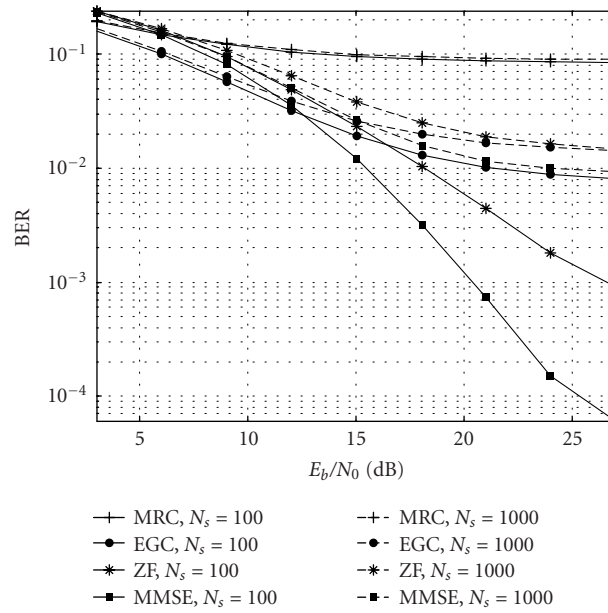

Figure 6: Performances results for configuration I, $N_u = 8$.

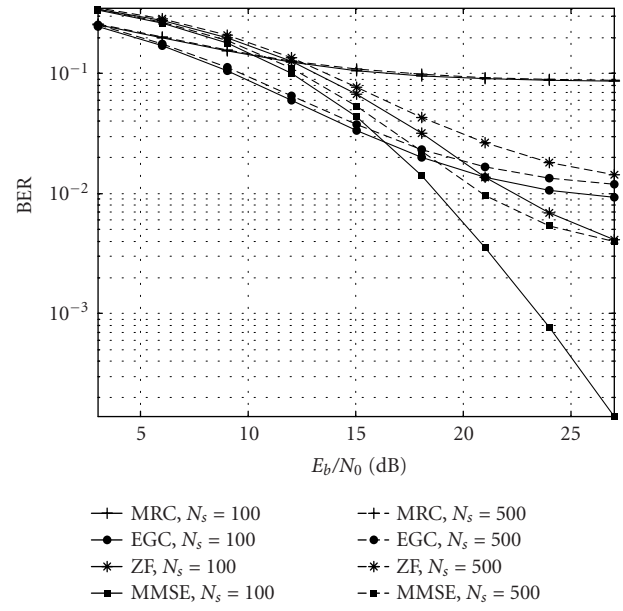

Figure 7: Performances results for configuration II, $N_u = 32$.

4. MODELISATION AND COMPLEXITY ANALYSIS EVALUATION

4.1. Modelisation step

In our design approach and according to specifications given Section 3, the CoMES methodology and its associated tool is used to firstly model the studied MC-CDMA system without any assumption about the architecture. The benefits of this approach is that the model will both be used for functional and architectural descriptions at an abstract level to ease HW-SW distribution and to evaluate implementation performances. The functional model is based on three complementary viewpoints [23]:

(i) the structural organisation viewpoint, which represents data dependencies between functional elements, is firstly specified. At the functional level, data are exchanged through ideal FIFO (first-in first-out) communication ports;

(ii) the behavioral viewpoint defines the set of operations and their time order for each function. These two complementary specifications are graphically defined;

(iii) the algorithm viewpoint is finally specified in C/C++ language and describes the set of instructions for each operation previously defined.

This description approach leads to an efficient design with reduced errors propagation and to a fully executable model for system verification and performances evaluation. The estimation of system performances uses an

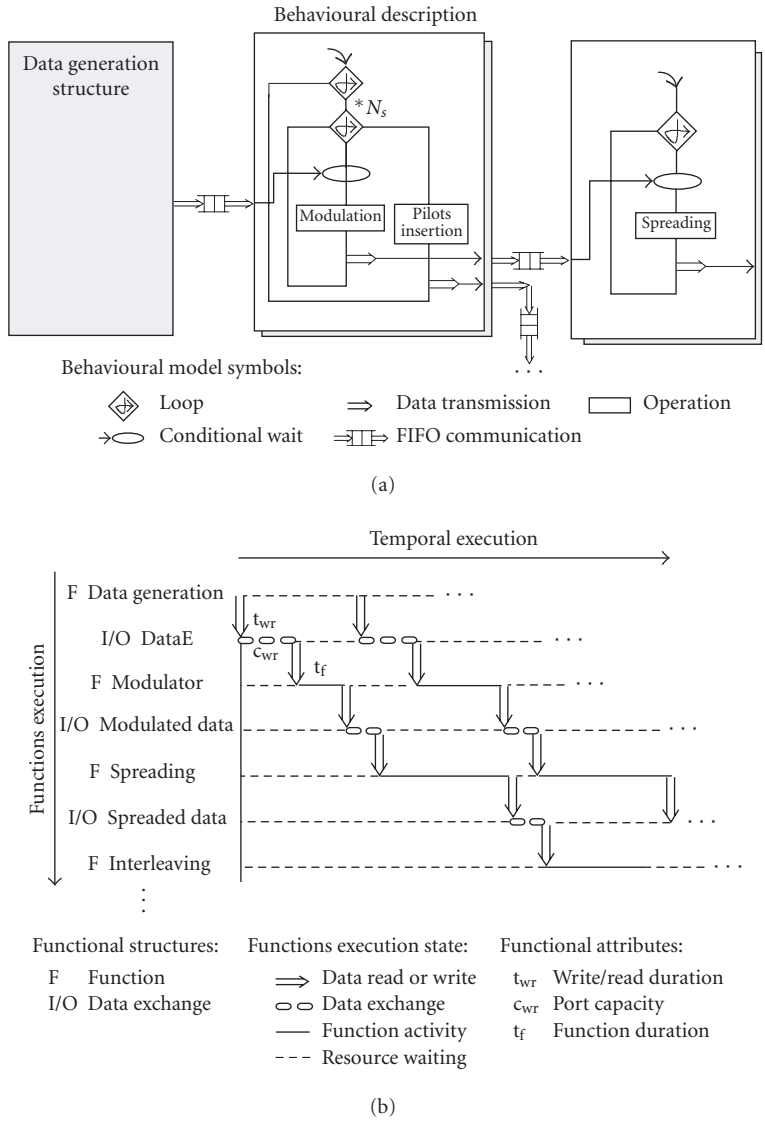

Figure 8: Example of (a) the MC-CDMA system modelisation and (b) execution graph representation according to associated functional attributes.

uninterpreted model, taking into account system attributes such as operation durations, data exchange formats, FIFO capacity, and so forth. The CoMES simulation model is then a true timed model and not only a functional model as used by most of commercial simulators. To illustrate system attributes influence, Figure 8 shows an MC-CDMA system modelisation example and the associated execution graph at the functional level. At this step, attributes can be set by default and will be more accurately determined once the functions durations evaluation step is done.

Figure 9 illustrates CoMES tool system simulation capabilities at the structural viewpoint and at the algorithm viewpoint. Moreover, generic parameters such as spreading length, number of users, or equalisation techniques can be set before simulation to obtain a flexible description and to ease design space exploration.

Then, the MC-CDMA system could fully be modeled using the CoMES tool. Besides, BER simulations were performed to validate system behaviour and used algorithms. This modelisation and functional validation is the first step to achieve before function complexity analysis.

4.2. Complexity analysis evaluation

Complexity analysis step aims at defining each function complexity and at investigating implementation performances according to the processor target kind. From system modelisation and specified algorithms, the CoMES tool allows to evaluate functions activity and relative complexity thanks to a profiling step. Complexity comparison illustrated in Figure 10 indicates relative functions duration in system execution. Channel model description complexity has not been represented. This step makes it possible to improve functions

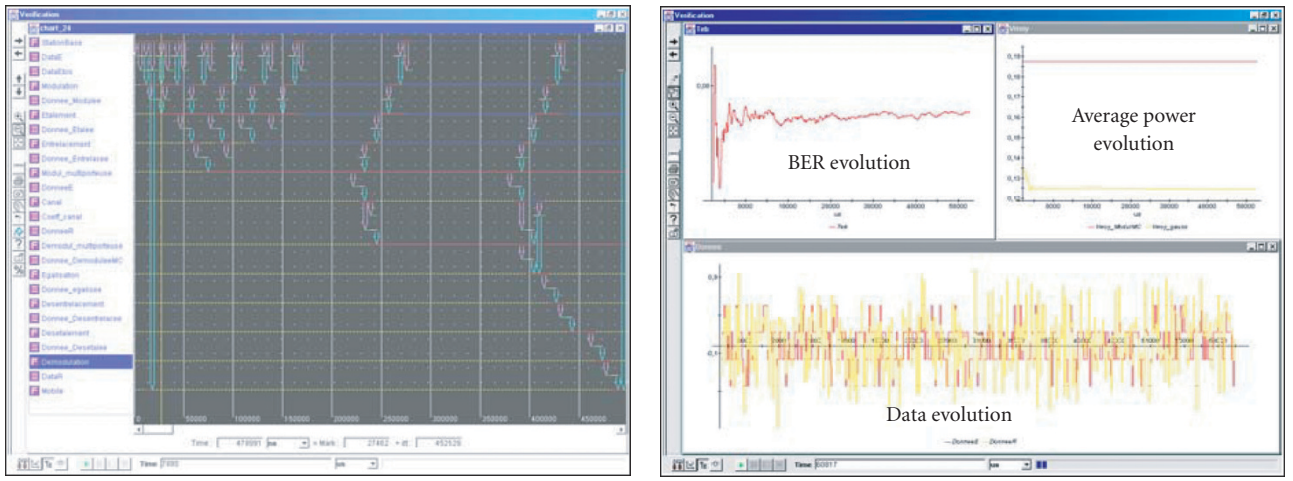

Figure 9: Example of system simulation applying the CoMES methodology and using the associated tool. On the left-hand side, the structural simulation is based on an execution graph representation of functions activity, and on the right-hand side, algorithmic simulation capabilities are presented.

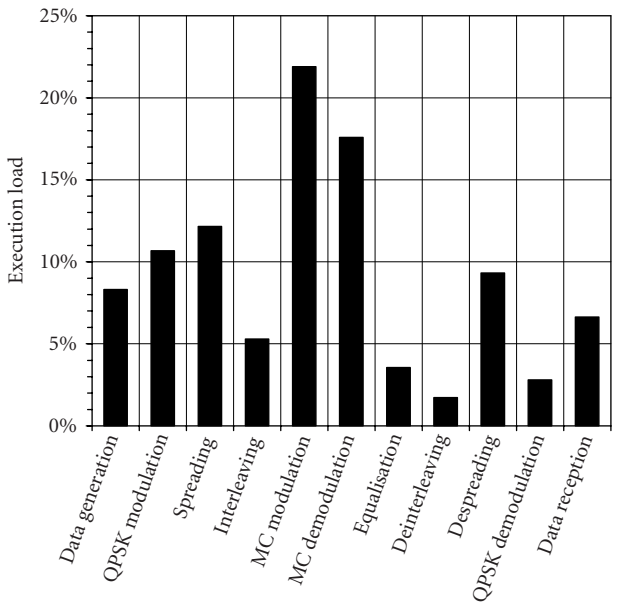

Figure 10: Function complexity evaluated for MC-CDMA configuration using $N_u = 32$ and $N_c = 256$.

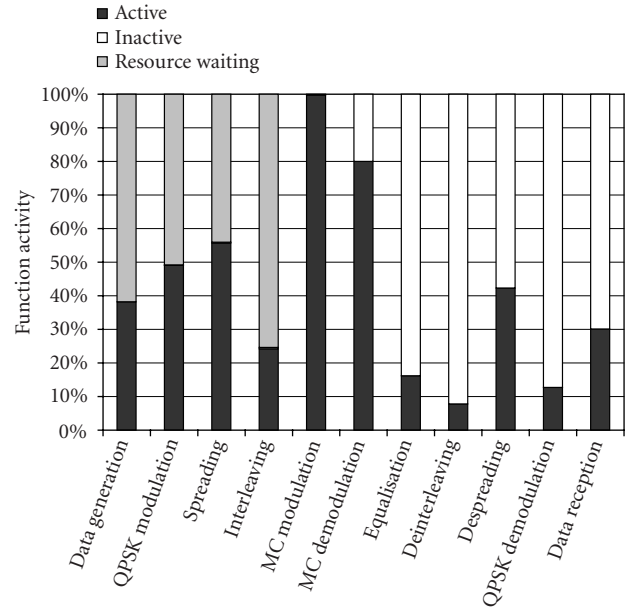

Figure 11: Functions activity in system execution evaluated for MC-CDMA configuration using $N_u = 32$ and $N_c = 256$.

description and coding style still without any architectural assumption.

Besides, each function activity can also be measured. Figure 11 illustrates the potential bottleneck represented by MC modulation and demodulation compared to other functions. Then, this function still remains the most computing function in the considered MC-CDMA system.

This profiling step helps designers to identify critical computing functions. In addition, for accurate architectural design, we completed this complexity evaluation by considering functions implementation performances according to processors targeted on our testbed platform [24]. Thus, whereas OFDM modulation is efficiently performed by an inverse fast fourier transform (IFFT) algorithm, spreading can conveniently be implemented using a fast hadamard transform (FHT).

Results given in Table 4 highlight benefits of FPGA implementation for most of the considered MC-CDMA functions. Computation times are measured according to C6701 DSP clock, that is, 6 nanoseconds, and considering a 20 nanoseconds cycle for the FPGA.

These values measured by implementation of each elementary function on the testbed components are used in order to find an efficient matching of MC-CDMA system on the architecture and to evaluate performances achievable with such a platform.

Table 4: Function implementation results in microseconds.

Parameters	Parameters set	C6701 DSP implementation	FPGA implementation
QPSK modulation	$N_c = 64, 256$	0.9, 3.5	0.96, 3.84
Spreading	$N_u = 4, 8, 16, 32, 64$	0.642, 1.542, 3.624, 8.274, 18.684	0.08, 0.16, 0.32, 0.64, 1.28
Interleaving	$N_c = 64, 256$	1.1, 4.2	0.96, 3.84
OFDM modulation	$N_c = 64, 256$	28.7, 146.718	3.84, 15.36
Channel estimation	$N_c = 64, 256$	0.7, 2.4	Not implemented
Equalisation	$N_c = 64, 256$	1.37, 4.83	3.84, 15.36

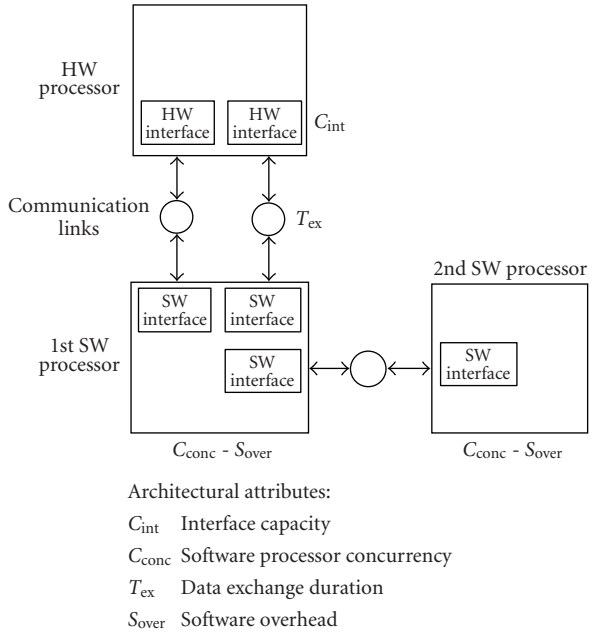

Figure 12: Architecture model using CoMES methodology.

5. ARCHITECTURAL DESIGN AND IMPLEMENTATION RESULTS

5.1. *Architectural design: functions distribution study and implementation efficiency evaluation*

The purpose of the architectural design step is to define an efficient matching between the developed functions and the available architecture. The CoMES methodology allows to study the impact of functions distribution on the architecture. Architectural attributes such as SW component concurrency, cycle duration for each component, SW overhead, and intercomponent communications durations complete the architecture description. We then modeled our platform as illustrated in Figure 12.

Nevertheless, despite the fact that the CoMES tool is still used as the performances evaluation method, the AAA methodology is followed to ease the distribution step. Indeed, this method and its associated tool SynDEx makes possible a quasiautomatic distribution and scheduling of the defined system on the architecture, taking into account previous evaluated functions durations and communication costs. Heuristic research is done to reduce system execution cycle. An example of function distribution and scheduling on the target architecture is illustrated in Figure 13.

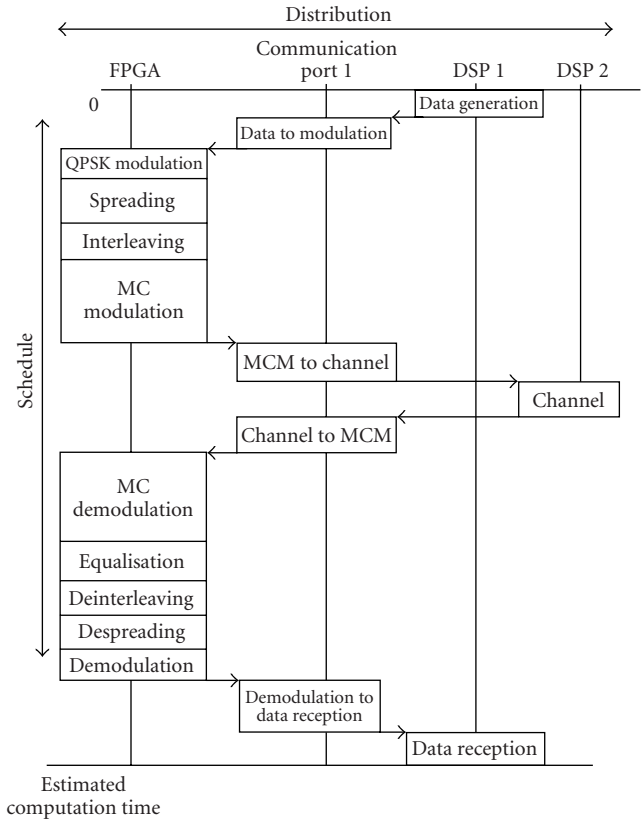

Figure 13: Matching exploration result.

Thanks to this exploration step, different distribution performances can easily be investigated, improving the difficult task of HW-SW partition. The retained solution can then be more accurately evaluated in the CoMES tool in terms of pipelined behaviour. The concurrent simulation of algorithms allocated on the architecture makes it possible, on the one hand, to optimize the target architecture or, on the other hand, to evaluate implementation performances at an abstract level. Then, achievable throughputs according to the architecture configuration can then be evaluated. Table 5 gives examples of simulation results following the CoMES methodology. The ideal case denotes results obtained neglecting the communication ports influence. Others cases takes into account the communication kind. It illustrates poor efficiency of a fully SW implementation and the potential bottleneck represented by intercomponent communications.

Table 5: Implementation performances evaluation per user.

Parameters		Configuration I $N_u = 8, N_c = 64$	Configuration II $N_u = 32, N_c = 256$
Fully SW implementation	Ideal	181 Kbps	36.4 Kbps
	Slow port	93.9 Kbps	31.4 Kbps
	Quick port	167 Kbps	35.8 Kbps
HW-SW implementation	Ideal	2.9 Mbps	780 Kbps
	Slow port	444 Kbps	125 Kbps
	Quick port	2.5 Kbps	645 Kbps

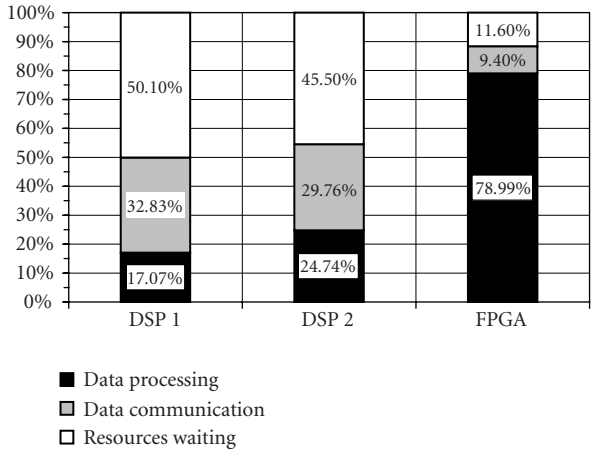

Figure 14: Component activity estimation for configuration II, $N_u = 32$, implemented on HW-SW architecture with quick ports.

Finally, the components activity can be measured for the most satisfactory solution, as illustrated in Figure 14 for the HW-SW implementation using quick ports.

Before implementation on the testbed platform, the last step of the design process is the generation of the codes both for the SW and the HW parts.

5.2. Hardware-Software code generation and implementation results

As indicated in Figure 3, the AAA methodology is used in order to generate codes at once for the SW, the HW part, and the interfaces. The code generation process is described in Figure 15. After the distribution step, the tool SynDEx makes it possible to generate distributed executives for each component. This code takes into account intercomponent synchronisations and calls to functions. The code generation uses specific libraries built according to the component kind. The description of theses libraries will not be addressed in the present paper, the reader should be refered to works described in [25].

The benefits of this approach are the generation of fully validated codes reducing the verification step once implementation on the testbed is done. The libraries used for SW generation already exist [26]. We built the needed library for HW generation [27]. This library uses the different developed functions and the required interfaces. The main synthesis results in terms of FPGA logic elements for each function implemented in the HW part are given in Table 6.

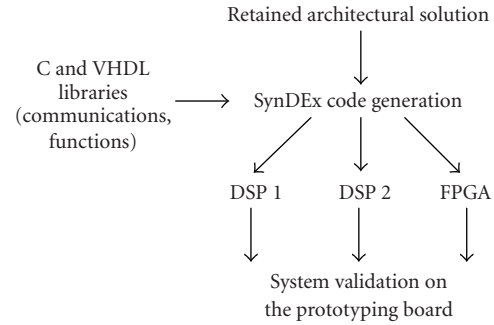

Figure 15: SynDEx code generation process.

For example, in the Configuration I case, the automatic generation of the HW part of the transmitter retained solution, both for the required interface and the computation functions, corresponds to 1132 logic elements and 12 memory blocks. Then, the HW synthesis results made it possible to fully validate this design at a 50 MHz frequency.

6. CONCLUSION

We have presented a codesign approach and associated tools for the MC-CDMA system rapid prototyping on a mixed architecture. This design goes from system specification and simulation to HW-SW code generation and implementation on a testbed platform. The use of the CoMES model allows system simulations at the functional level as well as at the architectural one. Then, this top-down design approach makes it possible to accurately evaluate system implementation efficiency, according to functions complexity and architecture properties. Finally, the use of the AAA methodology completes this HW-SW design by covering the distribution and code generation steps.

The described design process, applied to MC-CDMA system, facilitates and reduces the development cycle. Then, we easily investigate different implementation solutions according to the considered HW platform. Besides, the benefits of this approach fit into the SoftWare Radio (SWR) requirements for efficient design methods.

From our application's point of view, evaluation results and implementation show the ability to obtain high-speed data rate using a mixed architecture. The demonstrated

Table 6: Synthesis results in terms of occupied logic elements for the HW implemented functions.

Parameters	Configuration I	Configuration II
Spreading	138	400
Interleaving	143	325
OFDM modulation	590 – 6 memory blocks	655 – 6 memory blocks
Equalisation	200	315
Quick communication ports	80	80

feasibility of the studied MC-CDMA system could lead to its enhancement of the outdoor propagation characteristics.

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