EURASIP Journal on Applied Signal Processing 2004:13, 2066–2075

Analog-to-Digital Conversion Using Single-Layer Integrate-and-Fire Networks with Inhibitory Connections

Brian C. Watson
Department of Electrical and Computer Engineering, University of California, San Diego, La Jolla, CA 92093, USA
Email: bc7watson@adelphia.net

Barry L. Shoop
Department of Electrical Engineering and Computer Science, Photonics Research Center, United States Military Academy, West Point, NY 10996, USA
Email: barry-shoop@usma.edu

Eugene K. Ressler
Department of Electrical Engineering and Computer Science, Photonics Research Center, United States Military Academy, West Point, NY 10996, USA
Email: de8827@usma.edu

Pankaj K. Das
Department of Electrical and Computer Engineering, University of California, San Diego, La Jolla, CA 92093, USA
Email: das@cwc.ucsd.edu

Received 14 December 2003; Revised 6 April 2004; Recommended for Publication by Peter Handel

We discuss a method for increasing the effective sampling rate of binary A/D converters using an architecture that is inspired by biological neural networks. As in biological systems, many relatively simple components can act in concert without a predetermined progression of states or even a timing signal (clock). The charge-fire cycles of individual A/D converters are coordinated using feedback in a manner that suppresses noise in the signal baseband of the power spectrum of output spikes. We have demonstrated that these networks self-organize and that by utilizing the emergent properties of such networks, it is possible to leverage many A/D converters to increase the overall network sampling rate. We present experimental and simulation results for networks of oversampling 1-bit A/D converters arranged in single-layer integrate-and-fire networks with inhibitory connections. In addition, we demonstrate information transmission and preservation through chains of cascaded single-layer networks.

Keywords and phrases: spiking neurons, analog-to-digital conversion, integrate-and-fire networks, neuroscience.

1. INTRODUCTION

The difficulty of achieving both high-resolution and high-speed analog-to-digital (A/D) conversion continues to be a barrier in the realization of high-speed, high-throughput signal processing systems. Unfortunately, A/D converter improvement has not kept pace with conventional VLSI and, in fact, their performance is approaching a fundamental limit [1]. Transistor switching times restrict the maximum sampling rate of A/D converters. State-of-the-art high-frequency transistors have cutoff frequencies, f_T, of 100 GHz or more. Unfortunately, A/D converters cannot operate with multiple bit resolution at the limit of the transistor switching rates due to parasitic capacitance and the limitations of each architecture. There also exist thermal problems with A/D converters due to the high switching rates and transistor density. Electronic A/D converters with 4-bit resolution and sampling rates of several gigahertz have been achieved [2]. However, the maximum sampling rate for A/D converters with a more useful 14-bit resolution is 100 MHz. Presently, it is not possible to obtain both a wide bandwidth and high resolution, which limits the potential applications. A typical method for increasing the sampling rate is to use multiplexers to divert the data stream to multiple A/D converters. After data conversion, the binary data is reintegrated into a continuous data stream using a demultiplexer (see Figure 1). In

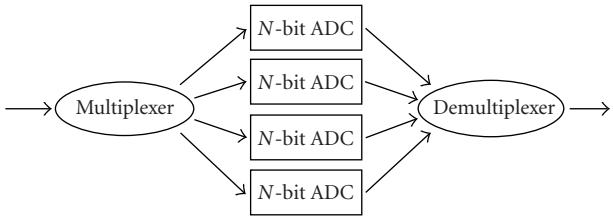


Figure 1: A typical scheme for increasing the sampling rate is to use multiple analog-to-digital converters in a mux-demux architecture. The performance of this architecture is limited by mismatch and to a lesser degree, timing error.

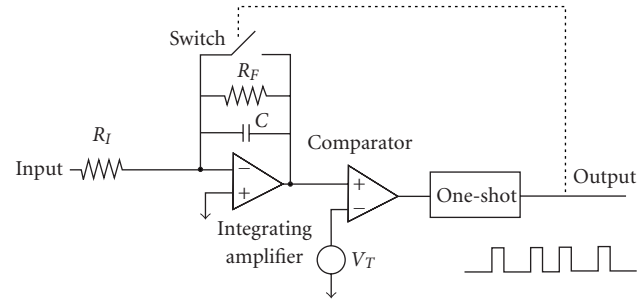


Figure 2: Representation of a single neuron using electronic components. The input is connected to an integrating amplifier. When the output of the integrating amplifier reaches a threshold defined by V_T, the comparator output changes to high. Subsequently, the one-shot produces an output pulse, which triggers the switch that grounds the amplifier voltage. This circuit operates asynchronously, analogously to a biological neuron.

theory, the sampling rate can be increased by a factor equal to the number of individual converters. In practice, the mismatch between each converter limits the performance of such systems. To minimize the effects of timing error, the multiplexers are usually implemented using optical components. Although recent advances in optical switches and architectures may improve the performance of A/D converters, it will be many years before commercial optical or hybrid converters are available.

Recently, innovative approaches to A/D conversion motivated by the behavior of biological systems have been investigated. The ability of biological systems with imprecise and slow components to encode and communicate information at high rates has prompted interest in the communication and signal processing community [3, 4, 5].

An analogy can be made between biological sensory systems and electronic A/D converters. Sensory organs are basically translating continuous analog input into a digital representation of that information. The primary difference being that all biological sensors rely on neurons to detect and transmit information. The operation of a single neuron is relatively simple. Neurons receive signals from the environment and other neurons through branched extensions, or dendrites, that conduct impulses from adjacent cells inward toward the cell body. A single nerve cell may possess thousands of dendrites, which form connections to other neurons through synapses. The aggregate input current from all of these other cells is accumulated (integrated) by the soma (cell body). Once the accumulated charge on the neuron reaches a threshold value, it fires, releasing a voltage pulse down its axon, which is usually connected to many other neurons. To continue the analogy, an output pulse corresponds to a binary "one." Although the amount of information that a single neuron can transmit is limited to a single bit, networks of spiking neurons are able to transmit relatively large signal bandwidths by modulating the collective timing of their output pulses [6, 7].

Compared to electronic components, neurons are decidedly imperfect. They operate asynchronously and have a limited firing rate of approximately 500 Hz [8]. The threshold voltage for each neuron is slightly different and even changes over time for a single neuron. In addition, neurons suffer from relatively large timing jitter compared to their firing rates. Given the limitations of a single neuron, it is remarkable that biological systems are able to perform A/D conversion so effectively. With our various senses, we are able to experience the environment in remarkable detail. Our sensory organs function even though neurons may be lost over time. In fact, the loss of neurons does not significantly degrade their performance.

Most importantly, the maximum sampling rate of a biological sensor system is not strictly limited by the firing rate of a single neuron. In fact, collections of neurons are able to conduct signals with bandwidths that are as much as 100 times larger than their firing rates. *This ability suggests that, in A/D converters of very high speed and precision, where electronic/photonic devices also appear slow and imprecise, neural architectures offer a path for advancing the performance frontier*.

2. ANALOGY BETWEEN NEURONS AND SIGMA-DELTA MODULATION

Each neuron can be thought of as an A/D converter and, in fact, a direct comparison can be made between a single neuron and a first-order 1-bit $\Sigma-\Delta$ modulator (see Figures 2 and 3) [9, 10]. The discrete time integrator, quantizer, and digital-to-analog converter (DAC) in Figure 3 can be represented by the integrating amplifier, comparator, and switch, respectively, in Figure 2. A $\Sigma-\Delta$ converter is a type of error diffusion modulator whereby the quantization noise produced by the converter is shifted to higher frequencies. In a $\Sigma-\Delta$ converter, for every doubling of the sampling frequency, we increase the signal-to-noise ratio (SNR) by 9 dB. We can compare this result to that obtained by just oversampling which provides 3 dB for every doubling of the sampling frequency. The noise shaping in $\Sigma-\Delta$ modulation evidently provides a significant SNR advantage over oversampling alone. This technique can also be extended to higher-order $\Sigma-\Delta$ architectures that employ second- or third-order modulators with the resulting decreased noise and increased circuit complexity. We can write the effective number of bits, b_{eff}, for an

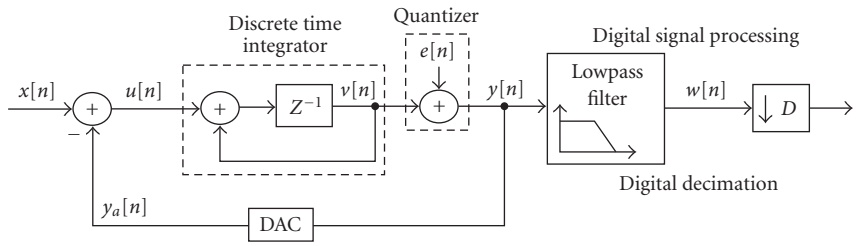


Figure 3: Block diagram of a first-order $\Sigma - \Delta$ modulator indicating the discrete time integrator, quantizer, and feedback path utilizing a digital-to-analog converter. The output data $y[n]$ is subsequently lowpass filtered and decimated by a digital postprocessor.

oversampled Nth-order $\Sigma - \Delta$ converter as

$$b_{\text{eff}} = \log_2 \left[\frac{\sqrt{2N+1}}{\pi^N} M^{(N+1/2)} \right], \tag{1}$$

where M is the frequency oversampling ratio [11]. An additional $N + 1/2$ bits of resolution are obtained for every doubling of the sampling frequency.

Due to the feedback, nonlinearities in the quantizer or the DAC will significantly degrade the noise performance of a $\Sigma - \Delta$ converter. Usually, to avoid these nonlinearities, $\Sigma - \Delta$ converters are operated with a resolution of only one bit, furthering the comparison between neurons and $\Sigma - \Delta$ A/D converters. In this case, the quantizer can be thought of as a comparator and the DAC as a switch. For a 1-bit $\Sigma - \Delta$ converter to have reasonable SNR, the oversampling ratio must be relatively large compared to the signal bandwidth. In general, 1-bit $\Sigma - \Delta$ modulators are operated at sampling rates that are at least a factor of a hundred larger than the signal bandwidth for audio applications.

Conversely, collections of neurons coordinated using feedback realize apparent sampling rates that are much larger than the sampling rate of an individual neuron. Clearly, the strength of the biological approach results from the collective properties of many neurons and not the action of any single neuron. The question remains, how do we organize multiple neurons to cooperate effectively?

3. SINGLE-LAYER INTEGRATE-AND-FIRE NETWORKS WITH INHIBITORY CONNECTIONS

3.1. Background

In a biological system, many neurons operate on the same input current in parallel, with their spikes added to produce the system output. Biological systems *do not* rely on a single neuron for A/D conversion. Because the same overall network-firing rate can be achieved with a lower *individual* neuron-firing rate, we would expect an advantage from using multiple neurons. However, in order to gain such an advantage, we must arrange for multiple neurons to cooperate effectively. Otherwise, neurons would fire at random times and occasionally; neurons would fire at approximately the same time. It has been hypothesized that feedback mechanisms in collections of neurons coordinate the charge-fire cycles. These neural connections cause temporal patterns in the summed output of the network, which result in enhanced spectral noise shaping and improved SNR[8].

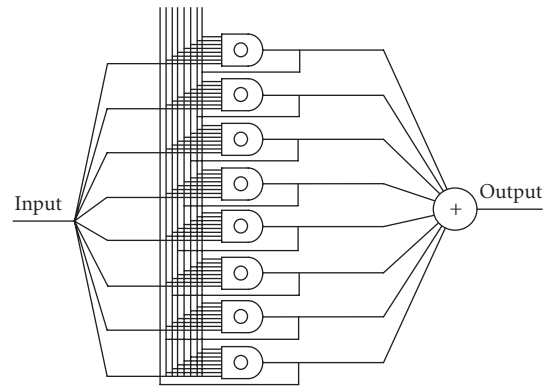


Figure 4: In a single-layer maximally connected network, the output of the network is subtracted from the input of every neuron. With sufficient negative feedback, this architecture insures that multiple neurons do not fire simultaneously.

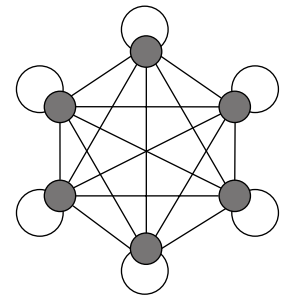


Figure 5: An alternative view of a maximally connected network. Each neuron (gray circle) is connected to all other neurons and to itself.

The most direct method (although not necessarily the optimal method) is to use negative feedback so that when a neuron fires, it inhibits nearby neurons from firing (Figures 4 and 5) [8, 12, 13]. An analogous negative feedback mechanism exists in biological systems, which is termed "lateral inhibition." In the retina of most organisms, for example, photoreceptors that are stimulated inhibit adjacent ones from firing. The overall effect is to enhance edges between light and dark image areas. This architecture also must be responsible for coordinating neurons so that the effective "SNR" of images that are received by the brain is increased.

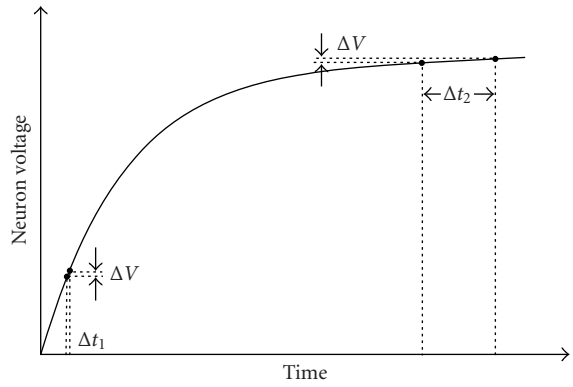


Figure 6: The regular spacing between firing times can be understood by considering the charge curve of the integrating amplifier. After any circuit in the network fires, a voltage, $\Delta V = K$, is subtracted from all other circuits. Although the voltage decrements are identical, each circuit experiences a different time setback depending on its position on the charge curve.

It may be apparent that the architecture in Figure 4 resembles the mux-demux architecture described at the beginning of this paper (see Figure 1). The major differences are:

(1) the circuit operates asynchronously. The timing between successive output spikes is determined by the self-organizational properties of the network. There is no need for precise timing and switching;
(2) mismatch between components does not appreciably degrade the network performance (each A/D converter uses only 1 bit). Due to the emergent behavior of the network, differences in the performance of each neuron actually improve the overall network performance. A certain amount of randomness in the system is necessary to avoid synchronization of neurons;
(3) loss or malfunction of a component or multiple components will produce a modest graceful (linear) degradation of the network performance. In typical (pulse code modulation) A/D converters, the loss or malfunction of any component immediately results in a complete failure of the system.

Without feedback to coordinate the individual neuron-firing times, the network output would comprise a Poisson process with a rate proportional to the instantaneous value of the input signal. For a fixed single neuron-firing rate, noise power would be uniformly distributed with total power proportional to the number of neurons and their base-firing rate [8, 14]. Negative feedback regulates the firing rate of the network so that firing times are evenly spaced, assuming a constant input. Hence, the spectrum of noise in the output spike train is shaped, leaving the low frequencies of the signal baseband comparatively noise-free. This noise shaping improves SNR substantially, just as it does in a $\Sigma - \Delta$ modulator.

The regular spacing between firing times can be understood by considering the charge curve of a particular integrating amplifier (see Figure 6). Because we have a leaky integrator (due to R_F, see Figure 2), the shape of the curve is increasing but concave downward. After any neuron in the network fires, a voltage, $\Delta V = K$, is subtracted from all other neurons. Although the voltage decrements are identical, each neuron experiences a different time setback depending on its position on the charge curve. Neurons that are almost ready to fire receive a larger time setback than those at the beginning of the charge curve. The overall result is to space the firing events evenly in time. We can also notice that after any neuron has fired, there is a refractory period during which all other neurons cannot fire. At the end of this refractory period, a spike occurs in any fixed time interval with uniform probability proportional to the network input voltage [15].

We have observed that, in simulations as well as breadboard prototypes, self-stabilization of a network of 1-bit A/D converters or neurons will occur spontaneously using specific sets of parameters. After which, the neurons will fire in a fixed order with each always following the same one of its peers. This condition is not an obvious outcome considering that we can apply any time dependent input signal to the network. In a previous paper, we have demonstrated through a deterministic argument that convergence to a stable state is guaranteed under certain initial conditions [15].

The network in Figure 4 is maximally interconnected so that after each neuron fires, it inhibits all other neurons from firing for a short time. For large numbers of circuits, this interconnection method may not be practical due to the wiring complexity. However, even if only nearby circuits are inhibited, this feedback architecture will still result in improved A/D converter performance [8].

3.2. Motivation

In designing an A/D converter consisting of a network of binary converters, we are primarily interested in the network-firing rate, the output noise, the signal-to-quantization noise ratio (SQNR), and the maximum input frequency. We have written equations for each of these parameters below. We are presently investigating harmonic performance (linearity) and intermodulation distortion although they are not discussed in this work.

3.3. Simulation details

We have modeled networks of maximally connected integrate-and-fire neurons depicted in Figures 2 and 4 using (2). In the simulations, we have used a temporal resolution of $\Delta = 1$ microsecond, which is approximately 100 times shorter than the time between output pulses, so that the circuit can be modeled as though it was operating asynchronously. The input is defined by a constant voltage V_C and a variable signal with an amplitude of V_S at a single frequency, f_0. In simulations, after the neuron reached the threshold voltage, V_T, its voltage was reset to zero. The simulations were run for two seconds and the first second of data was ignored. If multiple neurons fired during the same time interval, they were added together.

The output of the network consists of a train of spikes whose rate is modulated by the incoming signal. The output therefore has relatively small noise power at low frequencies and then a sudden increase in the noise spectrum

at frequencies near the output spike-firing rate (and its harmonics). Therefore, to operate as an A/D converter we must operate at input frequencies much less than the output spike-firing rate. We have defined a parameter, the noise-shaping cutoff frequency, f_{NS}, to describe the sudden increase in the noise spectrum power and thus the maximum input frequency as well.

The maximum network performance is achieved by using the shortest possible feedback signal. Longer time feedback signals correspond to uncertainty in the network-firing time and therefore reduce correlations between neuron output spikes. Since we are designing an A/D converter, and are thus interested in maximizing SQNR, the feedback signal used was always a square wave pulse. In the simulations, the pulse was always as short as possible (its length was equal to the temporal resolution of the simulation, $t_P = \Delta$).

3.4. Theory

The voltage on each neuron can be described by the following equation:

$$\frac{dV_i(t)}{dt} = -\frac{V_i(t)}{\tau_m} - \sum_{\substack{j=1 \\ j\neq i}}^{n} \sum_{m} \alpha_i K \delta\left(t - t_j^m\right) + \alpha_i (V_C + V_S(t)), \tag{2}$$

where $V_i(t)$ is the voltage on each neuron (output of each integrating amplifier), K is the feedback constant in volts, and t_j^m are the firing times for the jth neuron. The gain and the time constant of each integrating amplifier are defined as $\alpha = 1/R_I C$ and $\tau_M = R_F C$, respectively. The decay time constant of the amplifier, τ_M, is analogous to the membrane decay time constant of a neuron.

The firing rate and noise spectrum have been derived separately by Mar et al. [14] and Gerstner and Kistler [6]. In those papers, the average behavior of multiple neurons arranged in a network was treated analytically using a stochastic equation to describe the population rate. Using those results, we write an equation for the average network-firing rate as

$$F_N = \frac{n\alpha V_C}{V_T + t_P n K \alpha}. \tag{3}$$

If we assume that the quantization noise can be described by a Poisson process, we can estimate the quantization noise as $\sigma^2 = F_N \Delta$. If we limit our feedback to a pulse shape, using the results of Mar et al. [14] we can write the noise power spectrum as

$$P(f) = \frac{F_N \Delta}{\left|1 + (n\alpha K/\pi f V_T)\sin(\pi f t_p)\right|^2}. \tag{4}$$

This noise formula provides an overestimate of the quantization noise since the spacing between successive spikes can be extremely constant due to the network inhibition. However, given that the uniformity of the spike spacing is a function of the network stabilization and self-organization, it is difficult to write a general analytical expression for the noise.

Using (3), we can estimate the SQNR at low frequencies compared to the noise-shaping cutoff ($f_0 \ll f_{\mathrm{NS}}$) as

$$\begin{aligned} \mathrm{SQNR\,(dB)} &\approx 10 * \log\left[\frac{(\delta F_N)^2}{\sigma^2}\right] \\ &\approx 10 * \log\left[\frac{n^2\alpha^2 V_S^2}{(V_T + t_P n K \alpha)^2 (F_N \Delta)}\right], \end{aligned} \tag{5}$$

for n maximally connected neurons. From (3) and (5), we should expect an increase in the SQNR by using multiple neurons. The signal is proportional to n^2 while F_N, and therefore the noise, saturates above a critical number of neurons [14]. Therefore, the SNR increases first as n and then eventually n^2. To draw parallels with traditional A/D converter architectures, we could write the effective number of bits, b_{eff}, as

$$b_{\mathrm{eff}} \approx \frac{10 * \log\left[n^2\alpha^2 V_S^2/(V_T + t_P n K \alpha)^2 (F_N \Delta)\right] - 4.77}{6.02}. \tag{6}$$

From (4), we see that the noise power can be reduced by minimizing the pulse width t_p. In fact, it appears that for an infinitely small pulse width, the noise-shaping cutoff will be infinitely large. However, the noise floor is determined by (4) only at frequencies that are small compared to the noise-shaping cutoff frequency and hence the firing rate ($f_0 < f_{ns} \sim F_N$). The overall noise spectral density curve will be a combination of the noise from (4) and the noise power of the spike train harmonics. Thus, the noise floor is relatively flat until the noise-shaping cutoff frequency at which point the noise increases dramatically. If the feedback is large ($K > V_C/(t_P F_N)$), the noise-shaping cutoff frequency, f_{NS}, can be estimated as

$$f_{\mathrm{NS}} = F_N\left(1 - \left(\frac{V_S}{V_C}\right)\right). \tag{7}$$

If the inhibition is relatively small, every neuron will act independently and the noise-shaping cutoff frequency, f_{NS}, will approach

$$f_{\mathrm{NS}} = \frac{F_N}{n}\left(1 - \left(\frac{V_S}{V_C}\right)\right). \tag{8}$$

Hence, one of the primary advantages of the inhibition is to increase the bandwidth (maximum possible input frequency) of the network. We can also notice that if the variable part of the signal is equal to the constant input, $V_S = V_C$, then the noise-shaping cutoff is at zero frequency and the noise-shaping bandwidth is zero.

The simulated noise-shaping cutoff frequency f_{ns} versus the variable part of the input signal V_S is shown in Figure 7. The straight line represents the theory from (7). The vertical and horizontal axes have been scaled by the overall network firing rate and the constant portion of the input, respectively. We can understand (7), by considering the case where $V_S = 0$ (upper left portion of Figure 7). In this case,

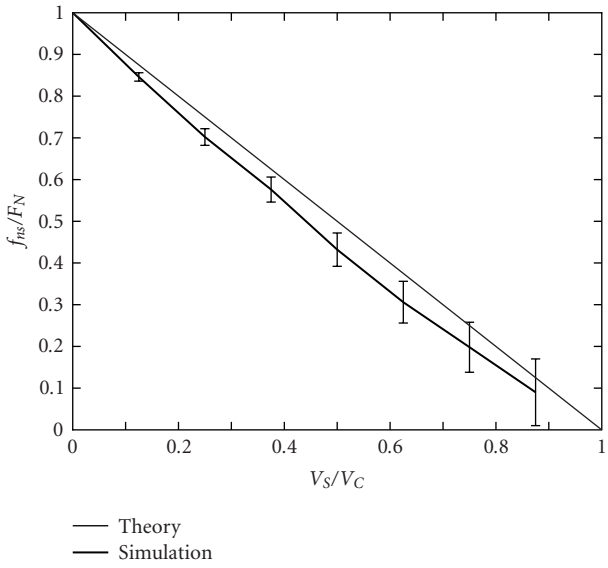


FIGURE 7: The simulated noise-shaping cutoff frequency f_{ns} versus the variable part of the input signal V_S. The straight line represents the theory from (7). The vertical and horizontal axes have been scaled by the overall network-firing rate and the constant portion of the input, respectively. The output spikes for individual neurons are not perfectly correlated, and hence the simulated curve approaches the theory from below ($n = 100$, $f_0 = 100\,\text{Hz}$, $V_C = 4\,\text{V}$, $V_T = 1\,\text{mV}$, $C = 1\,\mu\text{F}$, $R_I = 722\,\text{k}\Omega$, $R_F = 1\,\text{M}\Omega$, $t_P = \Delta = 1$ microsecond, $K = 5\,\text{kV}$).

the output consists of a constant train of spikes with all spikes equally spaced apart. The spectrum of such a spike train is defined by narrow peaks at the output-firing rate and its harmonics (since there is only a single temporal periodicity). The noise-shaping cutoff frequency is then equal to the firing rate. As we increase V_S, the time between successive spikes can vary over a range determined by V_S/V_C. Hence, the noise-shaping cutoff frequency is the inverse of the largest distance between successive spikes. However, in a network of multiple neurons, the feedback cannot perfectly organize the firing times and the time between each successive spike will vary slightly, that is, the output spikes for individual neurons are not perfectly correlated. Hence, the actual noise-shaping frequency cutoff will always be less than that given in (7) (in Figure 7, the simulated curve approaches the theory from below).

In fact, the SQNR will continue to increase as long as the time between firings is larger than the pulse width and the self-stabilization properties of the network are not compromised. The reason for the increased SQNR is straightforward; we are simply oversampling the signal by an increased rate, which is proportional to n. The oversampling rate of our network can be written as the frequency oversampling multiplied by the spatial oversampling, n.

$$\text{OSR} = \left(\frac{F_N}{f_B}\right) \cdot n, \tag{9}$$

where F_N is the firing rate of the network, f_B is the required signal bandwidth, and n is the number of neurons. We have demonstrated arbitrarily high SNRs in simulations by using shorter pulses and higher firing rates.

Although, using multiple neurons will increase the possible SQNR of the network, we could achieve the same effect by using a single-neuron circuit with a higher sampling rate. However, at high frequencies where conventional electronics are limited, increasing the sampling rate may not be possible.

3.5. Network leverage

The primary benefit of using a network of neurons is that the individual sampling rates can be lower than for a single neuron. If all of the neurons are firing, we expect that the maximum network input frequency is approximately equal to n times an individual neuron-firing rate. For example, consider the simulated power spectral density (PSD) for a single neuron with a 100 Hz sinusoidal input shown in Figure 8a. The firing rate, F_N, for this simulation was 5500 Hz and the SQNR was 75 dB. In Figure 8b, we have plotted the PSD for a network of 1000 neurons arranged with maximally connected negative feedback. The feedback value, K, had been adjusted so that the network operates at the same firing rate as the single neuron, 5500 Hz. However, the individual neuron-firing rates in the network were only 5.5 Hz. Amazingly, individual neurons firing at 5.5 Hz are able to process a signal as high as the noise-shaping cutoff of 2.4 kHz.

By using a network of 1000 *neurons, we have been able to achieve a network bandwidth that is* 2400/5.5 = 440 *times that of a single neuron!* At high frequencies, where electronic component speeds are limited by transistor switching rates and conventional electronics appear slow and imprecise, this architecture offers a method for increasing the maximum sampling rate. Conventional 1-bit A/D converters operate at sampling rates of up to 100 MHz. If we are able to coordinate multiple converters using feedback in an integrate-and-fire network, we should be able to achieve a network sampling rate approaching $n \times 100\,\text{MHz}$.

As with any circuit improvement, we pay a price in complexity. While the network sampling rate increases as n, the number of circuit interconnections increases as n^2. We will eventually reach a limit where the number of interconnections is not practical using VLSI. We note that the performance of a maximally connected network is only marginally superior to a locally connected network [8]. Therefore, it is not necessary for every neuron to be connected to every other neuron directly. However, the timing precision for each circuit must be maintained to obtain the SNR increases. The firing pulse delay and the pulse jitter will determine the minimum effective pulse width, t_p, that we can use. Fortunately, this system is relatively immune to timing jitter and inconsistencies in pulse sizes, and so forth. In fact, the system actually requires some randomness to operate, which is why in some simulations, we have set the gain to a distribution of values. If all of the randomness is removed, multiple neurons tend to synchronize resulting in nonlinear output and reduced noise shaping.

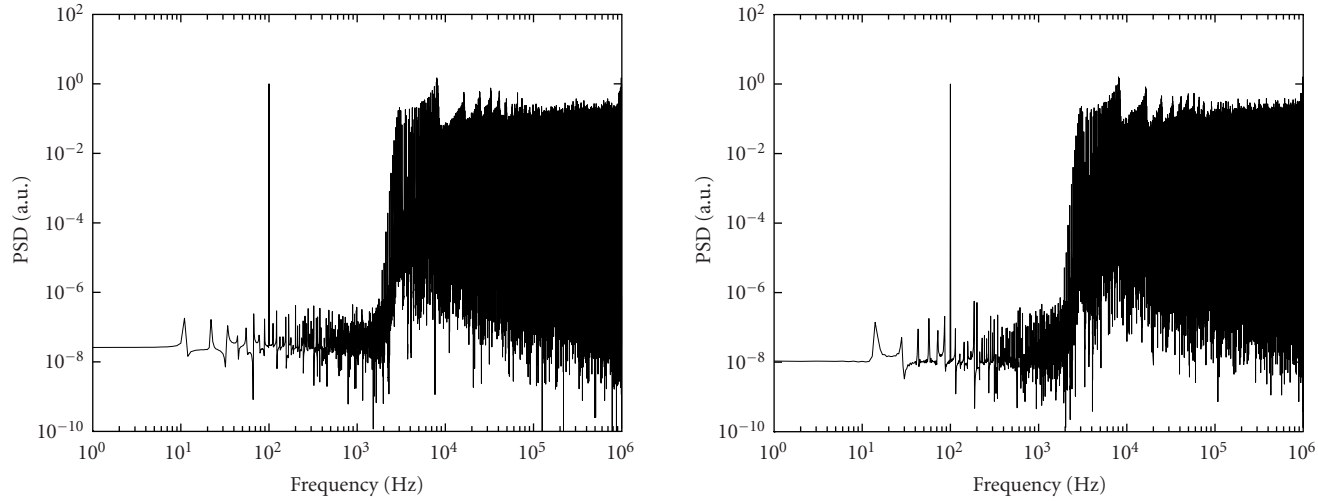


FIGURE 8: (a) The PSD for a single neuron with a 100 Hz sinusoidal input. The SQNR for this simulation was 75 dB and the firing rate was 5500 Hz. (b) The PSD for 1000 neurons with a 100 Hz sinusoidal input. The network-firing rate was 5500 Hz while the individual neuron-firing rate was only 5.5 Hz ($f_0 = 100$ Hz, $V_C = 4$ V, $V_S = 2$ V, $V_T = 1$ mV, $C = 1\,\mu$F, $R_I = 722\,$kΩ, $R_F = 1\,$MΩ, $t_P = \Delta = 1$ microsecond, $K = 5$ kV (b only)).

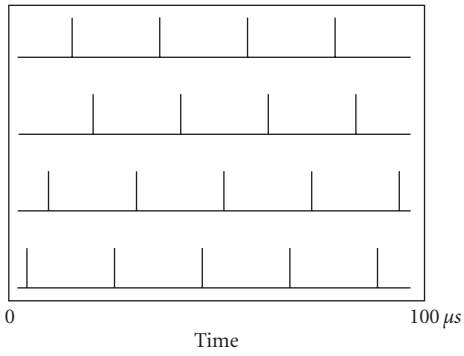


FIGURE 9: The *measured* output spike times for individual neurons in a four-neuron breadboard circuit operating at approximately a 200 kHz rate. The spikes are spaced out evenly due to the network self-organization.

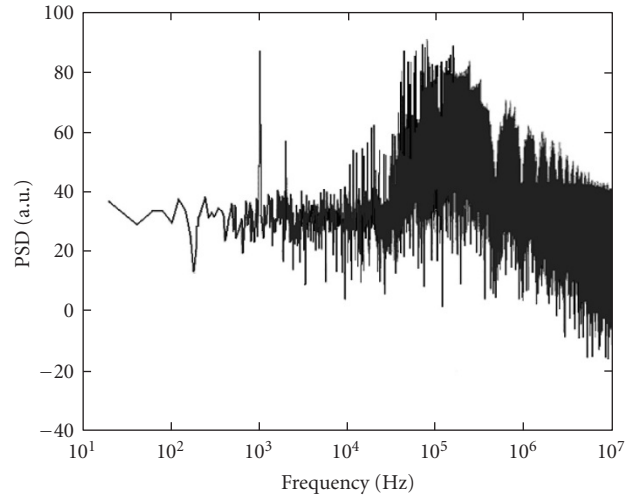


FIGURE 10: The measured power spectral density for a four-neuron breadboard network operating at approximately a 63.5 kHz rate ($f_0 = 1$ kHz, $V_C = 2$ V, $V_S = 1$ V, $V_T = 0.95$ V, $C = 220$ pF, $R_I = R_F = 120\,$kΩ, $t_P = \Delta = 1$ microsecond, K=25 V).

3.6. Experimental results

Thus far, we have constructed breadboard and printed circuit board prototypes with four 1-bit A/D converters coordinated using negative feedback. A single 1-bit A/D converter circuit consists of an integrator, comparator, one-shot, and analog switch. To simplify the design, we have used the idealized schematic in Figure 2 instead of the transistor circuit that is typically used [16, 17]. The integrator and comparator are based on the LF411 operational amplifier. Since the open loop gain of the amplifier determines the maximum sampling rate of each neuron, the LF411 operational amplifier will eventually be replaced by a more suitable component. The one-shot (or monostable multivibrator) and the analog switch (transmission gate or quad bilateral switch) are also both commercially available items. We have measured the output from our prototype boards using a PCI 6601 counter board and Labview software and are satisfied that it matches the expected performance from simulations. The measured output spike times for each individual neuron in a four-neuron breadboard circuit operating at approximately a 200 kHz rate is shown in Figure 9. The actual spike width was measured using an oscilloscope as approximately 2 microseconds. The even spacing between spikes is evidence of the self-organization of the network produced by the negative feedback. The PSD of the combined four-neuron output operating at a 63.5 kHz rate is shown in Figure 10. The noise-shaping cutoff is evident at approximately 40 kHz.

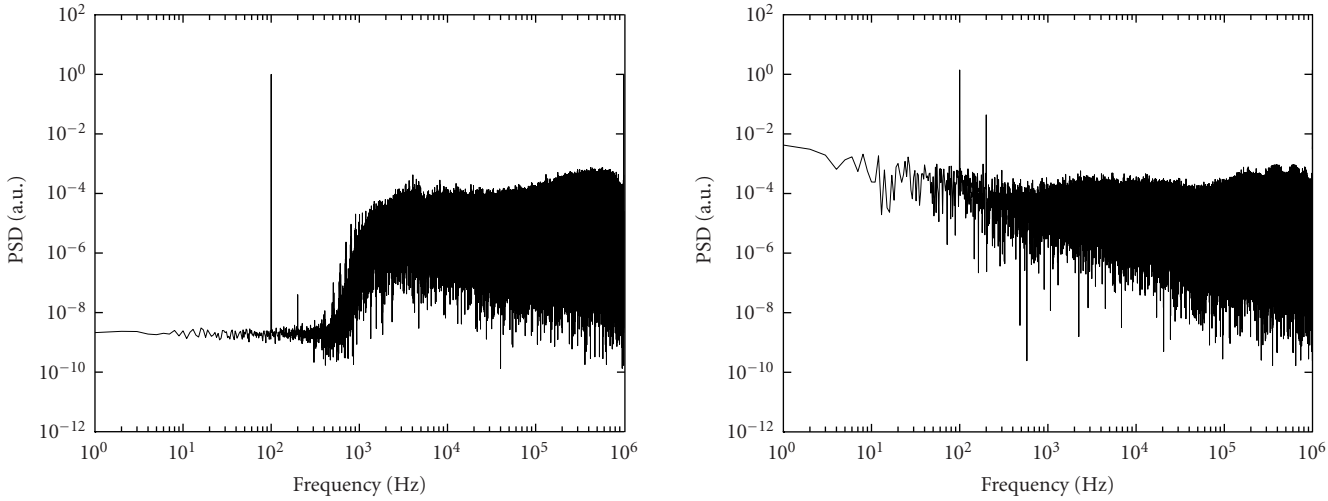


FIGURE 11: The power spectral density for the output of the first cascaded stage (a) and the fifth cascaded stage (b). Each stage consisted of 100 neurons arranged with maximally connected feedback. ($f_0 = 100$ Hz, $V_C = 4$ V, $V_S = 2$ V, $V_T = 1$ mV, $C = 1\,\mu$F, $R_I = [666\,\text{k}\Omega, 1\,\text{M}\Omega]$, $R_F = 1\,\text{M}\Omega$, $t_P = \Delta = 1$ microsecond, $K = 10$ V, gain between stages = 500.) The input resistor, R_I, was set to a uniform random variable over the range from 666 kΩ to 1 MΩ to discourage neuron synchronization.

The nonlinearities near 20 kHz are related to the parasitic capacitance between various elements on the breadboard. In fact, the major limitation to producing larger networks thus far is the parasitic inductance and capacitance due to the breadboard and the wire lengths used. We are currently designing printed circuit board prototypes that will allow us to combine as many as 100 1-bit A/D converter circuits in a network. The goal is to eventually construct VLSI networks with thousands of individual circuits on a single chip.

4. CASCADING NETWORKS

By connecting the output of a network of 1-bit A/D converters to the input of another stage, forming a chain, it is possible to cascade multiple networks together. In our simulations, we have kept the constant part of the signal, V_C, equal for each stage. The varying part of the signal amplitude, V_S, was multiplied by a gain of 500 after the first stage to prevent signal degradation. Since spikes are such short-time events, the gain is necessary for the output signal to affect the next stage. For these simulations, if two neurons spiked in the same time period, only one spike event was recorded.

It may seem apparent that the signal would be transmitted without loss given that, if we had added a lowpass filter after each stage, the input to each subsequent stage would be approximately the original first-stage input sine wave. However, since without filtering the output signal for each stage consists entirely of spikes, it is not obvious that we will be able to transmit information from stage to stage without loss.

The simulated PSD for the first (a) and fifth stage (b) of a cascaded chain with 100 1-bit circuits per stage is shown in Figure 11. By the fifth stage, most of the noise shaping has disappeared and the harmonics have increased. For this set of parameters, the SQNR diminished for the first few stages but then eventually reached an equilibrium where the SQNR remained constant for an unlimited number of stages. Interestingly, the spike pattern between stages is not identical. Analogously to biological systems, the information moves in a wave down the chain, where the output of each stage is only statistically coordinated with the output of previous stages [18]. However, if the gain is high enough, the pattern of output spikes will remain fixed.

5. SUMMARY

We are developing an A/D converter using an architecture inspired by biological systems. This architecture utilizes many parallel signal paths that are coordinated by negative feedback. With this approach, it should be possible to construct an electronic A/D converter whose overall sampling rate is comparable to the maximum transistor switching rate (100 GHz). The resolution of the converter will be limited only by the number of neurons that are able to operate collectively. Constructing an electronic device with hundreds of cooperating circuits will present novel engineering challenges. However, we have already constructed prototype circuits with four 1-bit A/D converters whose performance agrees with theoretical predictions.

Although the networks described thus far operate asynchronously, at some point we may want to analyze the output using a clocked digital signal processor. We have described possible methods for the integration of clocked circuits and asynchronous IF networks in a previous paper [15]. However, the eventual goal is to analyze the output of the integrate-and-fire network with another network of asynchronous neurons.

Up to this point, we have only considered first-order 1-bit A/D circuits due to their analogy with biological neurons. The noise-shaping frequency cutoff due to error diffusion can be increased by using higher-order neural circuits (see (1)). Unfortunately, individual higher-order integrate-and-fire circuits can become unstable [19, 20]. Nevertheless, we believe it is possible to cascade individual circuits to form a dual or multilayer network to obtain performance gains without incurring instability problems. We are currently pursuing investigation of higher-order A/D converters with negative feedback as well as variations of the basic architecture to improve network performance.

Cascading entire networks so that the output of one network becomes the input to the next network has shown that it is possible to transmit signals in this manner without loss of information and without filtering between the stages. Although the information contained in the rate coding of the spike output is preserved, the spike pattern that carries that information is different from stage to stage. Analogously to biological systems, the information is contained in the statistical correlations of the spike patterns.

We have demonstrated that it is possible to develop a high-speed A/D converter with high-resolution using networks of imperfect 1-bit A/D converters. The architecture utilizes many parallel signal paths without relying on serial-to-parallel switching circuits (mux-demux). Instead, the network self-organization produced by global inhibition engenders cooperation between circuits so that the sampling rate is increased and the noise shaping and SQNR are significantly enhanced.

ACKNOWLEDGMENT

We are grateful to Trace Smith, Tai Ku, Jason Lau, and Gary Chen for their invaluable assistance with both the simulation and experimental work.

REFERENCES

[1] B. L. Shoop and P. K. Das, "Mismatch-tolerant distributed photonic analog-to-digital conversion using spatial oversampling and spectral noise shaping," *Optical Engineering*, vol. 41, no. 7, pp. 1674–1687, 2002.

[2] B. L. Shoop and P. K. Das, "Wideband photonic A/D conversion using 2D spatial oversampling and spectral noise shaping," in *Multifrequency Electronic/Photonic Devices and Systems for Dual-Use Applications*, vol. 4490 of *Proceedings SPIE*, pp. 32–51, San Diego, Calif, USA, July 2001.

[3] R. Sarpeshkar, R. Herrera, and H. Yang, "A current-mode spike-based overrange-subrange analog-to-digital converter," in *Proc. IEEE Symposium on Circuits and Systems*, Geneva, Switzerland, May 2000, http://www.rle.mit.edu/avbs/.

[4] Y. Murahashi, S. Doki, and S. Okuma, "Hardware realization of novel pulsed neural networks based on delta-sigma modulation with GHA learning rule," in *Proc. Asia-Pacific Conference on Circuits and Systems*, vol. 2, pp. 157–162, Bali, Indonesia, October 2002.

[5] W. Gerstner, "Population dynamics of spiking neurons: fast transients, asynchronous states, and locking," *Neural Computation*, vol. 12, no. 1, pp. 43–89, 2000.

[6] W. Gerstner and W. M. Kistler, *Spiking Neuron Models*, Cambridge University Press, Cambridge, Mass, USA, 2002.

[7] W. Maass and C. M. Bishop, *Pulsed Neural Networks*, MIT Press, Cambridge, Mass, USA, 2001.

[8] R. W. Adams, "Spectral noise-shaping in integrate-and-fire neural networks," in *Proc. IEEE International Conference on Neural Networks*, vol. 2, pp. 953–958, Houston, Tex, USA, June 1997.

[9] J. Chu, "Oversampled analog-to-digital conversion based on a biologically-motivated neural network," M.S. thesis, UCSD School of Medicine, San Diego, Calif, USA, June 2003.

[10] P. M. Aziz, H. V. Sorensen, and J. V. D. Spiegel, "An overview of sigma-delta converters," *IEEE Signal Processing Magazine*, vol. 13, no. 1, pp. 61–84, 1996.

[11] B. L. Shoop, *Photonic Analog-to-Digital Conversion*, Springer Series in Optical Sciences, Springer-Verlag, New York, NY, USA, 2001.

[12] D. Z. Jin and H. S. Seung, "Fast computation with spikes in a recurrent neural network," *Phys. Rev. E*, vol. 65, 051922, 2002.

[13] D. Z. Jin, "Fast convergence of spike sequences to periodic patterns in recurrent networks," *Phys. Rev. Lett.*, vol. 89, 208102, 2002.

[14] D. J. Mar, C. C. Chow, W. Gerstner, R. W. Adams, and J. J. Collins, "Noise shaping in populations of coupled model neurons," *Proc. Natl. Acad. Sci. USA*, vol. 96, pp. 10450–10455, 1999.

[15] E. K. Ressler, B. L. Shoop, B. C. Watson, and P. K. Das, "Biologically motivated analog-to-digital conversion," in *Applications and Science of Neural Networks, Fuzzy Systems, and Evolutionary Computation VI*, vol. 5200 of *Proceedings SPIE*, pp. 91–102, San Diego, Calif, USA, August 2003.

[16] J. T. Marienborg, T. S. Lande, and M. Hovin, "Neuromorphic noise shaping in coupled neuron populations," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 5, pp. 73–76, Scottsdale, Ariz, USA, May 2002.

[17] C. Mead, *Analog VLSI and Neural Systems*, Addison Wesley, Menlo Park, Calif, USA, 1989.

[18] P. Reinagel, D. Godwin, S. M. Sherman, and C. Koch, "Encoding of visual information by LGN bursts," *Journal of Neurophysiology*, vol. 81, pp. 2558–2569, 1999.

[19] K. Uchimura, T. Hayashi, T. Kimura, and A. Iwata, "VLSI-A to D and D to A converters with multi-stage noise shaping modulators," in *Proc. IEEE Int. Conf. Acoustics, Speech, Signal Processing*, vol. 11, pp. 1545–1548, Tokyo, Japan, April 1986.

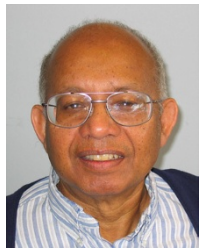
[20] T. Hayashi, Y. Inabe, K. Uchimura, and T. Kimura, "A multistage delta-sigma modulator without double integration loop," in *IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, vol. 29, pp. 182–183, February 1986.

Brian C. Watson attended the University of Illinois at Urbana-Champaign and graduated with a Bachelor's degree in electrical engineering in 1990. After graduation he worked for the Navy and Air Force as an Electronics Engineer. In the fall of 1996, he began school at the University of Florida, and finished his Ph.D. degree in physics in December, 2000. The topic of his thesis was magnetic and acoustic measurements on low-dimensional magnetic materials. The primary purpose was to understand the quantum mechanical mechanism governing high temperature superconductivity. During his time at University of Florida, he also designed and built a 9-Tesla nuclear magnetic resonance system that can operate at temperatures near 1 K. Due to his novel approach to problem solving, he was awarded the University

of Florida Tom Scott Memorial Award for Distinction in Experimental Physics. He is currently employed as a Research Scientist for Information Systems Laboratories. In his spare time, he mentors students in circuit design at the Electrical and Computer Engineering Department at the University of California at San Diego.

Barry L. Shoop is Professor of electrical engineering and the Electrical Engineering Program Director at the United States Military Academy, West Point, New York. He received his B.S. degree from the Pennsylvania State University in 1980, his M.S. degree from the US Naval Postgraduate School in 1986, and his Ph.D. degree from Stanford University in 1992, all in electrical engineering. Professor Shoop's research interests are in the area of optical information processing, image processing, and smart pixel technology. He is a Fellow of the OSA and SPIE, Senior Member of the IEEE, and a Member of Phi Kappa Phi, Eta Kappa Nu, and Sigma Xi.

Eugene K. Ressler is an Army Colonel and Deputy Head of the Department of Electrical Engineering and Computer Science at the United States Military Academy. He formerly served as Associate Dean for Information and Educational Technology at West Point. He is a 1978 graduate of the Academy and holds a Ph.D. degree in computer science from Cornell University. His military assignments include command in Europe and engineering staff work in Korea. Colonel Ressler's research interests include neural signal processing and computer science education.



Pankaj K. Das received his Ph.D. degree in electrical engineering from the University of Calcutta in 1964. From 1977 to 1999, he was a Professor at the Rensselaer Polytechnic Institute, NY. Currently, he is an Adjunct Professor at the Department of Electrical and Computer Engineering, University of California, San Diego, where he teaches electrical engineering. In addition, to his teaching duties, he directs individual research groups formed from combinations of faculty and students that study novel electrical engineering and data acquisition concepts. Professor Das has published 132 papers in refereed journals and 185 papers in proceedings. He is the author of two books, coauthor of three books, and has contributed chapters in five other books. He is the coinventor listed on four patents with the last one issued on March 4, 2003 entitled "Photonic analog to digital conversion based on temporal and spatial oversampling techniques."