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# Asynchronous analog-to-digital converter based on level-crossing sampling scheme

Mohammadmehdi Kafashan\*, Sajjad Beygi and Farrokh Marvasti

## Abstract

In this paper, a new iterative algorithm is used to convert analog signals to digital (A/D) using an asynchronous A/D converter. It is a realtime system, which encodes the amplitude information of the analog signal into a time sequence. In particular, using asynchronous systems for data conversion is an effective technique in order to reduce power consumption. The decoder should recover original signal from irregular samples. If a more intelligent reconstruction technique is used for decoding, signals with higher bandwidth can be digitized. In this work, we employ delta- and sigma-delta level-crossing sampling schemes. These asynchronous A/D converters are simple to implement and have very good performance with lower power consumption.

**Keywords:** signal reconstruction, analog-to-digital converter, level-crossing sampling, iterative algorithm

## 1 Introduction

Analog-to-digital converters have many applications in digital signal processing and communication systems. Conventional A/D converters consist of two steps: sampling operation followed by digital quantization. The noise introduced by signal distortion due to quantization decreases the A/D performance. In the literature, the performance of A/D converters is measured by the number of bits per sample and signal-to-noise ratio (SNR) [1,2].

Uniform sampling is used for synchronous implementation where a common clock is operated in order to convert analog signals to digital values. In the sigma-delta modulator, the original signal is highly over-sampled and the internal clock operates at a much higher rate than the bandwidth of the signal; however, the oversampled signal down-sampled at the last stage of A/D converter. On the other hand, most of the signals generated by temperature sensors, pressure sensors, electro-cardiograms and speech signals are almost always constant and may vary significantly for only brief moments [3,4]. Thus, conventional converters using uniform sampling at the Nyquist rate are limited in the implemented signal bandwidth, but asynchronous

converters can be used in order to decrease the internal clock rate.

Asynchronous converters can be implemented without a global clock and have interesting properties, such as low power consumption and reduction of electromagnetic interferences. A nonuniform sampling scheme is used for this aim. In this process, several reference amplitude levels are considered in the dynamic range of the input signal. A sample must be taken only when a reference level is crossed. In this case, samples are not spaced regularly, and the sampling rate depends on the input signal. In other words, when the input signal become active, the sampling rate is increased and vice versa. In the level-crossing scheme, two sets of the time instant and amplitude levels of the samples are saved. This sampling scheme is the dual of the uniform sampling, where the time instants are quantized, while the amplitudes are perfectly known [5-9].

In this paper, a new class of A/D converters based on the level-crossing scheme is investigated. Asynchronous delta- and sigma-delta modulation are analyzed in order to minimize the activity, decrease the power consumption of the converters and achieve a good SNR. The next section describe synchronous and asynchronous A/D converters in relation to the iterative decoding algorithm. In sections 3 and 4, the new contributions of this paper are presented, and finally Section 5 concludes this paper.

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## 2 Basic principles

### 2.1 Synchronous A/D converter

In synchronous converters, uniform samples quantized to approximate a continuous range of values by a specific set of discrete values. The quantization process incurs loss of information in the reconstructed signal. Subsequently, the reconstructed signal may differ considerably from the original analog signal. In order to overcome this problem, we must use oversampling converters. In the oversampling converters, sampling rate is greater than Nyquist rate ( $f_{\text{Nyquist}} = 1/\tau_{\text{Nyquist}}$ ). The ratio between the sampling rate and twice the signal bandwidth is defined as the oversampling ratio (OSR). After oversampling, the signal is subject to quantization and then low-pass filtered and finally down-sampled to or near to the Nyquist rate (known as decimation) [10].

The two main types of oversampling converters are delta modulators (DM) and sigma-delta modulator (SDM). The SDM is a kind of A/D converter derived from delta modulation. The principle of the sigma-delta architecture is to make rough evaluations of the signal, to measure the error, and then integrate and compensate for that error [11]. In SDM converter, we have following equation

$$x_n - q_n = \Delta^m u_n \quad (1)$$

which  $x$  is our original analog signal and  $q$  is the output of A/D converter. Here,  $\Delta$  is the difference operator, which can be defined by  $\Delta u_n = u_n - u_{n-1}$ . We have defined auxiliary sequence  $u$  as the state sequence. This explicit factorization of the quantization error is useful if  $u$  is a bounded sequence. It means that SDM, which is determined from (1), is unstable and impractical unless the sequence  $u$  is bounded. The relation (1) is valid for  $n > 0$ , and we consider  $u_n = 0$  for  $n < 0$  (this state is an initial condition for a recursive relation (3)). In practice, the sequence  $u$  can be obtained by integrating the difference equation (1) based on an associated "quantization rule,"

$$q_n = Q(u_{n-1}, u_{n-2}, \dots, x_n, x_{n-1}, \dots) \quad (2)$$

Consequently, the output bit stream  $q_n$  can be generated by using (2), and the sequence  $u$  can be expressed as

$$u_n = \sum_{k=1}^n (-1)^{k-1} \binom{m}{k} + u_{n-k} + x_n - q_n \quad (3)$$

The mathematics of sigma-delta A/D conversion is extremely challenging. Here, we use following difference equation to introduce an SDM scheme of order  $m$ .

If we consider one-bit quantizer as the quantization rule, the auxiliary sequences  $u$  can be achieved from the

following relation

$$u_n = u_{n-1} + x_n - \text{sign}(u_{n-1} + x_n) \quad (4)$$

In order to have a bounded sequence  $u$ ,  $y$  and  $q$  must not be unrelated sequence because  $u$  is determined from  $y - q$  via (1). Therefore,  $Q$  must be such to tie  $q$  to  $y$  to control  $u$ .

### 2.2 Asynchronous A/D converter

In asynchronous converters, we deal with nonuniform sampling and the original signal should be reconstructed from two sets of time instants ( $t_k$ ) and the corresponding amplitude values. Nonuniform sampling using level-crossing method is shown in Figure 1. In this type of converter, the time difference between irregular samples should be quantized and transmitted. Therefore, we need a local timer instead of an amplitude quantizer, and the quality of the A/D converter is related to the precision of local timer ( $T_c$ ). By reducing the value of  $T_c$ , the SNR of the reconstructed signal can be improved.

There are many methods to reconstruct the original signal from nonuniform samples. Reconstruction can be performed by using the TV<sup>a</sup> method [12], the lagrange method [13] and the CFT<sup>b</sup> method [14]. Suppose that ( $t_k, k \in \mathbb{Z}$ ) are increasing time instants of an irregular samples. Subsequently, nonuniform samples  $x_s(t)$  can be written as  $x_s(t) = \sum_{i \in k} x(t_i) \delta(t - t_i)$ . The sampling set ( $x_{t_k, k \in \mathbb{Z}}$ ) should be a stable sampling set. This means that this set of samples uniquely determines signal  $x(t)$  and, for this reason, the relation  $\int |x(t)|^2 dt \leq C \sum_i |x(t_i)|^2$  should be satisfied, where  $C$  is a constant. For instance, if  $|t_k - k\tau| < (\tau/4)$ , the set is stable ( $\tau$  is the Nyquist sampling rate).

The iterative method is used in order to recover the original signal  $x(t)$  from its nonuniform samples,  $x_s(t)$  [15]. The block diagram of an iterative algorithm is shown in Figure 2. In this scheme,  $G$  is a distortion operator (it is known from the modulator and demodulator that caused the distortion in the input signal). The iterative algorithm is given by

$$x_{k+1}(t) = x_0(t) + (I - G)x_k(t) \quad (5)$$

where  $x_{k+1}(t)$  is the  $k$ th iteration and  $x_0(t)$  can be any function of time. However,  $x_0(t) = G(x(t))$  is a good choice to achieve faster convergence. In general,  $G$  can be either a linear or nonlinear operator. By defining the operators  $\hat{G} = \lambda G$  and  $E = I - \hat{G}$ , we can rewrite (5) as

$$x_{k+1}(t) = \hat{G}(x(t)) + (I - \hat{G})x_k(t) \quad (6)$$

where  $\lambda$  is the relaxation parameter that determines the convergence rate. It is simple to express  $x_k(t)$  as

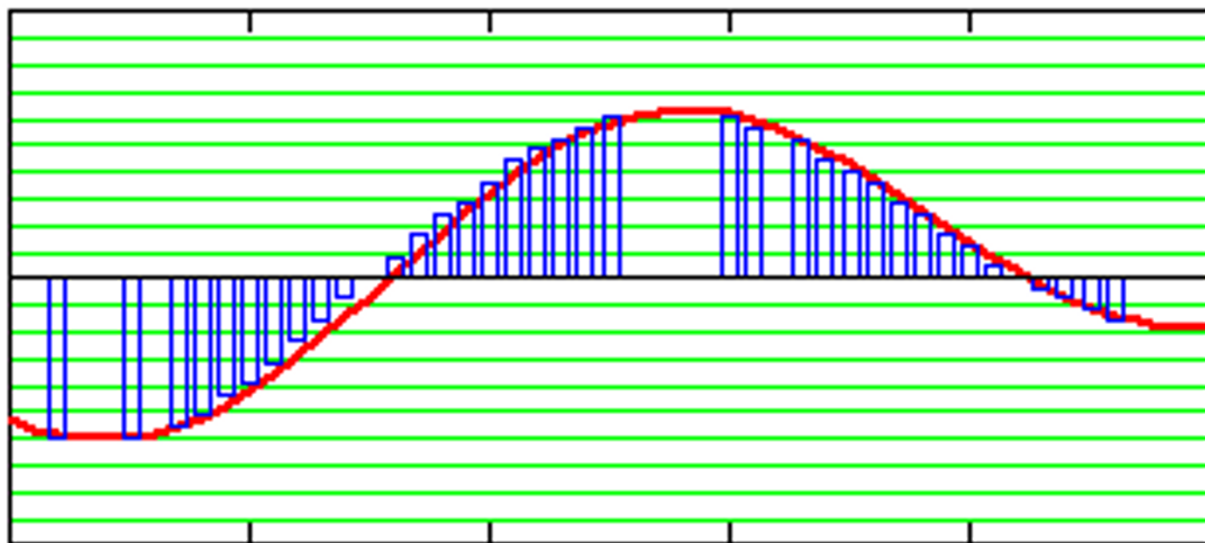


Figure 1 Nonuniform sampling using level crossing method.

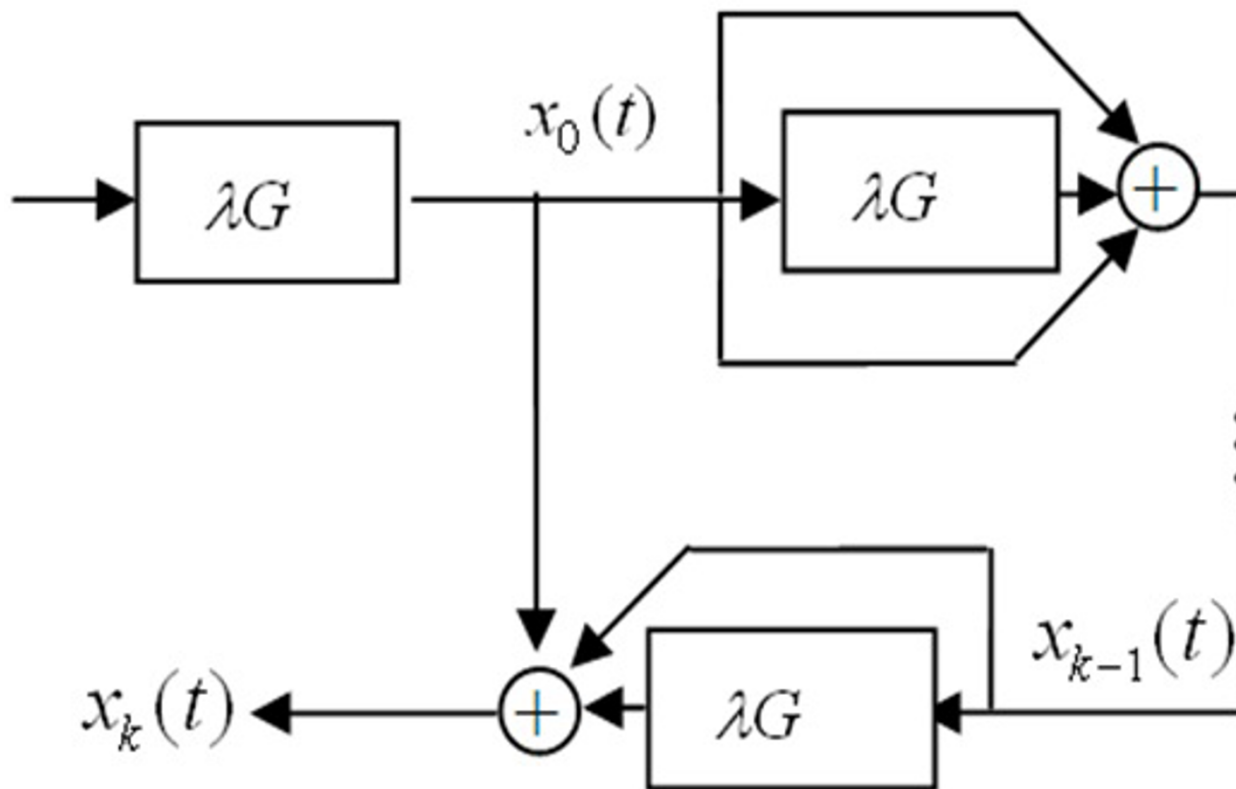


Figure 2 The configuration of iterative method.

$$x_k(t) = (E^k + E^{k-1} + \dots + E + 1) \tag{7}$$

If  $G$  is considered as a linear operator, then we have the following relation

$$E^k + E^{k-1} + \dots + E + 1 = \frac{I - E^{k+1}}{I - E} \tag{8}$$

If the norm of operator  $E$  satisfies  $\|E\| < 1$ , by increasing the number of iterations  $k$ , (6) approaches the inverse system  $\hat{G}$  (as it is shown in (8)); therefore,  $x_k(t)$  converges to  $xt$ .

In our problem concerning the signal from nonuniform samples, distortion operator of  $G$  is an interpolator and a low-pass filter. Nonuniform samples pass from an interpolator in order to uniform, and then, a low-pass filter is used to remove the high frequency of the output of the interpolator. The SNR of reconstructed signal is dependent on the order of low-pass filter. the iterative method is a good idea to improve A/D performance without using a complicated filter.

The convergence rate of the iterative method can be increased by using the Chebyshev acceleration (CA) algorithm. The block diagram of this method is shown in Figure 3. The convergence rate of the conventional iterative method is low even for the optimum parameter. By using the CA method, we can improve the iteration algorithm with relatively little additional complexity. The acceleration method can be stated as

$$x_n = \lambda_n \left( x_1 + x_{n-1} - \frac{2}{A+B} G(x_{n-1}) - x_{n-2} \right) + x_{n-2} \tag{9}$$

where  $x_0 = G(x(t))$  and  $x_1 = \frac{2}{A+B} x_0 G$  is the distortion operator, which is defined in the previous section. In order to obtain a good performance,  $A$  and  $B$  must be chosen properly (they have to be selected by numerically). Also,  $\lambda_n$  can be determined as follows:

$$\lambda_n = \left( 1 - \frac{\rho^2}{4} \lambda_{n-1} \right)^{-1} \tag{10}$$

where  $\rho$  is expressed as

$$\rho = \frac{B - A}{B + A} \tag{11}$$

The iterative method is used to improve the performance of synchronous A/D converters, too. In the case of synchronous SDM converters, distortion operator ( $G$ ) comprise of a sigma-delta modulator and a low-pass filter (LPF) to remove the shaped quantization noise. The block diagram of operator  $G$  for a first-order sigma-delta modulator is shown in Figure 4.

### 3 Asynchronous delta modulator

In an asynchronous A/D converter based on level-crossing scheme, the conversion of samples takes place whenever a reference level is crossed. The number of reference levels depends on the dynamic range of the continuous input signal. In delta level-crossing converters, difference between the input signal and the output of the converter is passed from a level-crossing sampler. In this case, the dynamic range of the input of the level-crossing sampler and, consequently, the number of

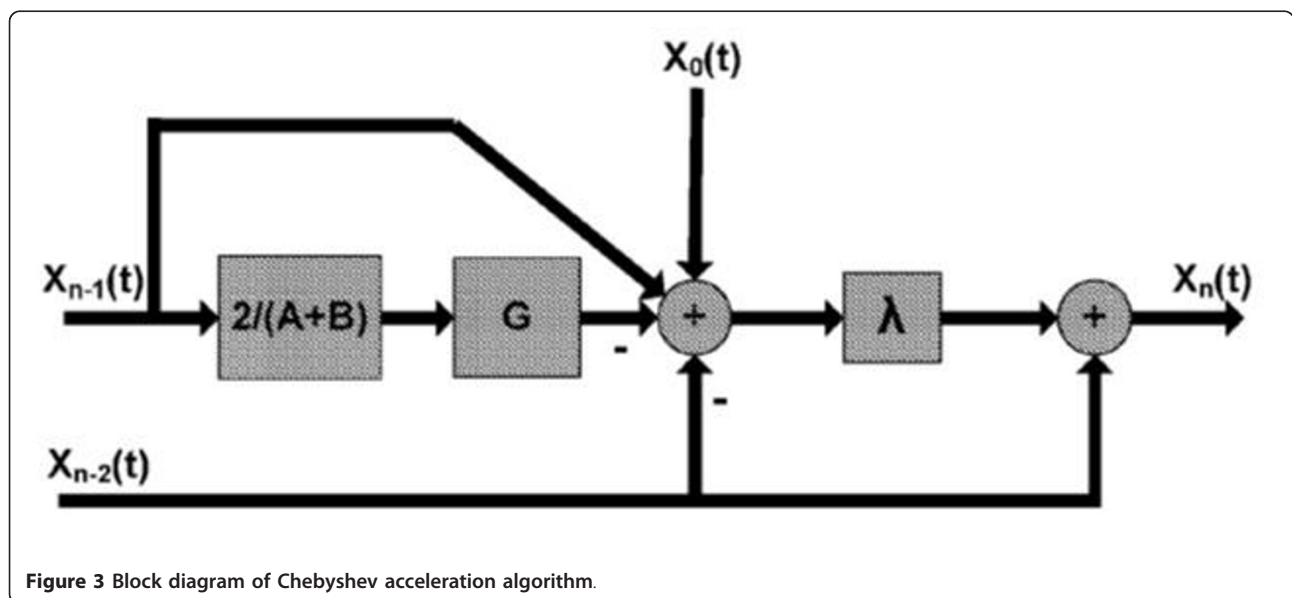
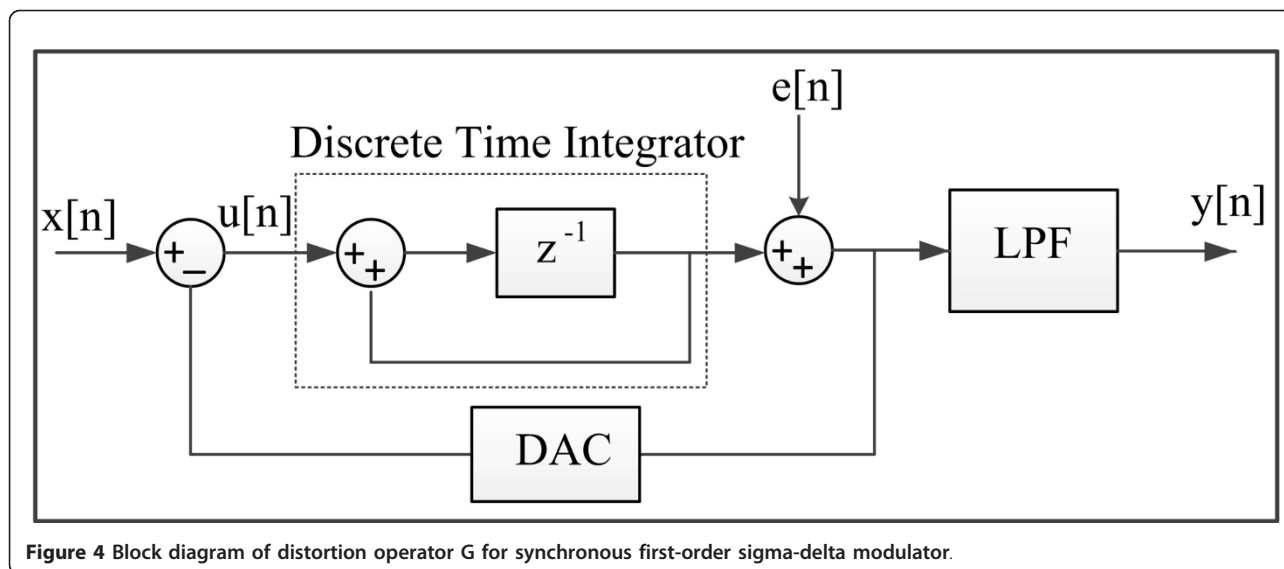


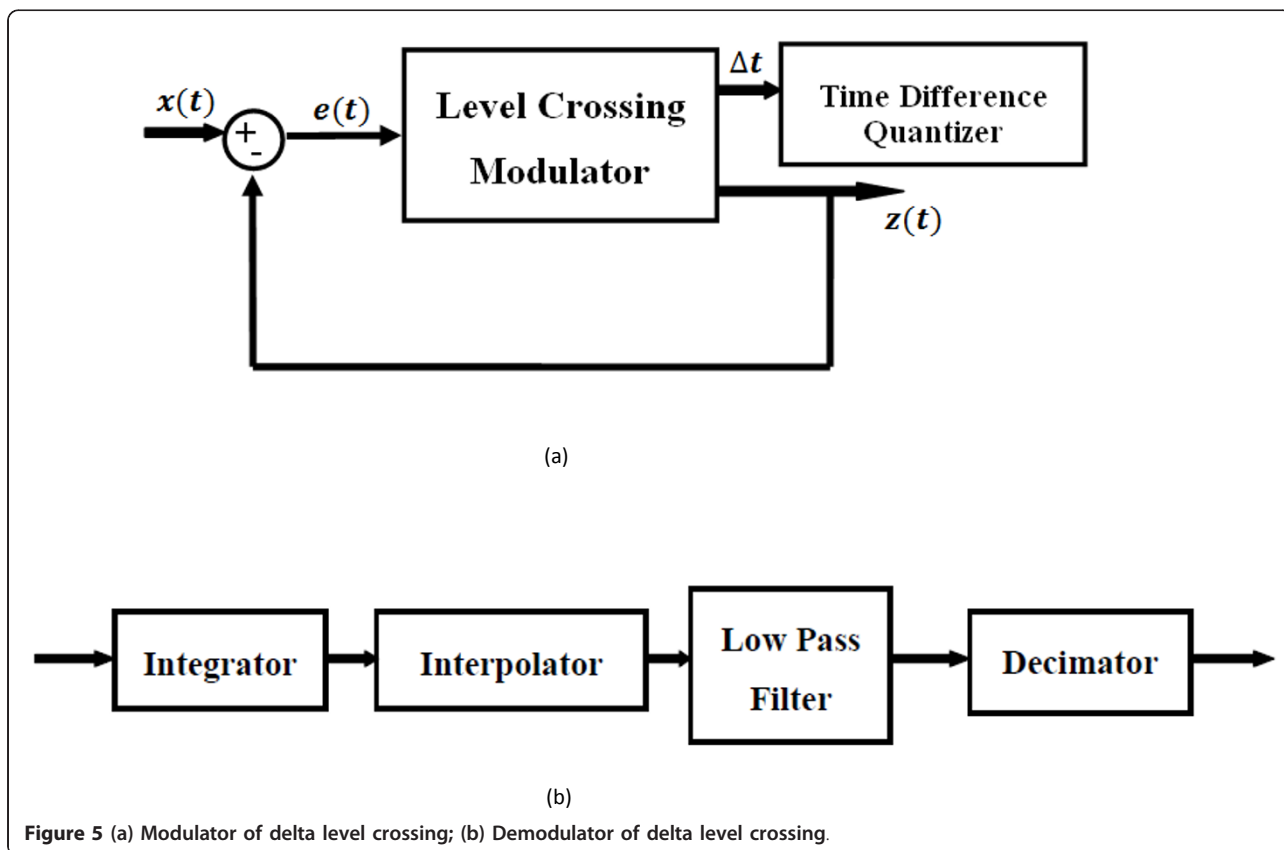
Figure 3 Block diagram of Chebyshev acceleration algorithm.



reference levels is decreased. Therefore, the number of bits that are allocated to the amplitude of the input signal is reduced. The amplitude and time of each converted sample should be considered for digital transmission. The time difference between two consecutive samples is quantized instead of the time of each sample in order to prevent quantization error

propagation. In asynchronous DMs, the dynamic range of the input signal should be known in order to specify the number of reference levels and determine the interval between them.

The modulator of asynchronous DMs is shown in Figure 5a. Reconstruction of the original signal from the output of the modulator is depicted in Figure 5b. As



can be seen in this figure, the nonuniform sampling obtained from the level-crossing sampler is passed from an integrator. The integrator assumes that irregular samples are uniform, and then, integration is performed. Subsequently, the output integrator, which is a set of nonuniform samples, is passed from the interpolator, and uniform samples are achieved. The approximation of the original input signal is obtained by applying a low-pass filter to the output of interpolators in order to suppress the high-frequency components of the interpolated signal. A decimator is used at the final stage to reduce the sampling rate to the Nyquist rate.

The SNR of asynchronous DM is the same as the SNR which is derived in [4]. Suppose that  $\delta t$  is the error of time quantization. Then, the amplitude error of reconstructed signal will be  $\delta V$ , which can be derived from the input signal and  $\delta t$  [16] with the following: equation

$$\delta V_1 = \frac{dV_1}{dt} \cdot \delta t \quad (12)$$

In Equation (12),  $V_1$  is the input of the level-crossing sampler, which is obtained from a delta modulation scheme, and  $\frac{dV_1}{dt}$  is its slope. The quantization noise power  $P(\delta V_1)$ , in the case that  $\frac{dV_1}{dt}$  and  $\delta t$  are considered as independent random processes, can be obtained from the following formula:

$$P(\delta V_1) = P\left(\frac{dV_1}{dt}\right) \cdot P(\delta t) \quad (13)$$

In each time instant,  $V_1$  is the input analog signal  $V_{in}$  subtracted from a previously selected reference level. Therefore,  $\frac{dV_{in}}{dt}$  is equal to  $\frac{dV_1}{dt}$  and SNR for asynchronous delta modulation can be written as

$$\text{SNR}_{dB} = 10 \cdot \log\left(3 \frac{P(V_{in})}{P\left(\frac{dV_{in}}{dt}\right)}\right) + 20 \cdot \log\left(\frac{1}{T_c}\right), \quad (14)$$

where  $P(V_{in})$  and  $P\left(\frac{dV_{in}}{dt}\right)$  are the power of the input signal and its derivation, respectively. The time difference of between consecutive samples is quantized according to the precision  $T_c$  timer. It can be understood from above equation that, by decreasing the value of  $T_c$  and increasing the precision of the time quantizer, the SNR of reconstructed signal will be increased.

In asynchronous converters, the oversampling ratio is not an integer number and depends on the statistical characteristics of the input signal. The SNR of the reconstructed signal versus the precision of the time

quantizer  $\left(\frac{1}{T_c}\right)$  for different over sampling rates is shown in Figure 6. In this figure,  $N$  is the number of bits for the amplitude quantizer (it specifies the interval between reference levels). It can be seen in this figure that, for a specific OSR, the SNR of the reconstructed signal is increased by increasing the frequency of the time quantizer  $\left(\frac{1}{T_c}\right)$ . After a threshold value for  $T_c$ ,

increase in the SNR is trivial. The same results (e.g., Figure 5) will be obtained for the level-crossing converter when the number of quantization bits is 9, 7 and 5. On the other hand, by using the delta level-crossing, the number of reference levels is decreased to 105 (7 bits), 25 (5 bits) and 7 (3 bits). The number of bits that are needed to encode the difference time of between samples for different timer resolutions  $\left(\frac{1}{T_c}\right)$  is shown in

Table 1. As expected, by increasing the sampling rate, the distance of between the samples is decreased and it causes a reduction in the number of reference levels (bits that are needed for amplitude quantizer).

The iterative algorithm is used in order to improve the performance of delta level-crossing converter. The distortion operator  $G$  consists of the modulator and demodulator of the delta level-crossing converter, excluding the decimator module in the demodulator. In this method, the optimal  $\lambda$  is obtained in way that the SNR in its saturate value after 10 iterations will be maximum. SNR versus the iteration number for three different timer resolutions is illustrated in Figure 7. It can be comprehended from this figure that for a specific timer resolution, the SNR of the reconstructed signal cannot be enhanced by increasing the number of iterations after a certain threshold. Hence, in order to improve the SNR of the reconstructed signal, the precision of time quantizer should be increased.

#### 4 Asynchronous sigma-delta modulator

The asynchronous sigma-delta modulator can be implemented without any clock and can operate at low supply power because of its asynchronous design and simple corresponding circuitry. In synchronous SDM A/D converters, a high dynamic range is achieved. However, there is a large number of coarsely quantized samples. By combining the SDM with the level-crossing scheme, the number of converted samples is decreased and a high dynamic range is obtained. The modulator of this converter consists of an integrator and a level-crossing sampler in a negative feedback loop.

The concept of this A/D converter is presented in Figure 8. As can be seen in Figure 8b, an interpolation stage converts nonuniform samples from the level-



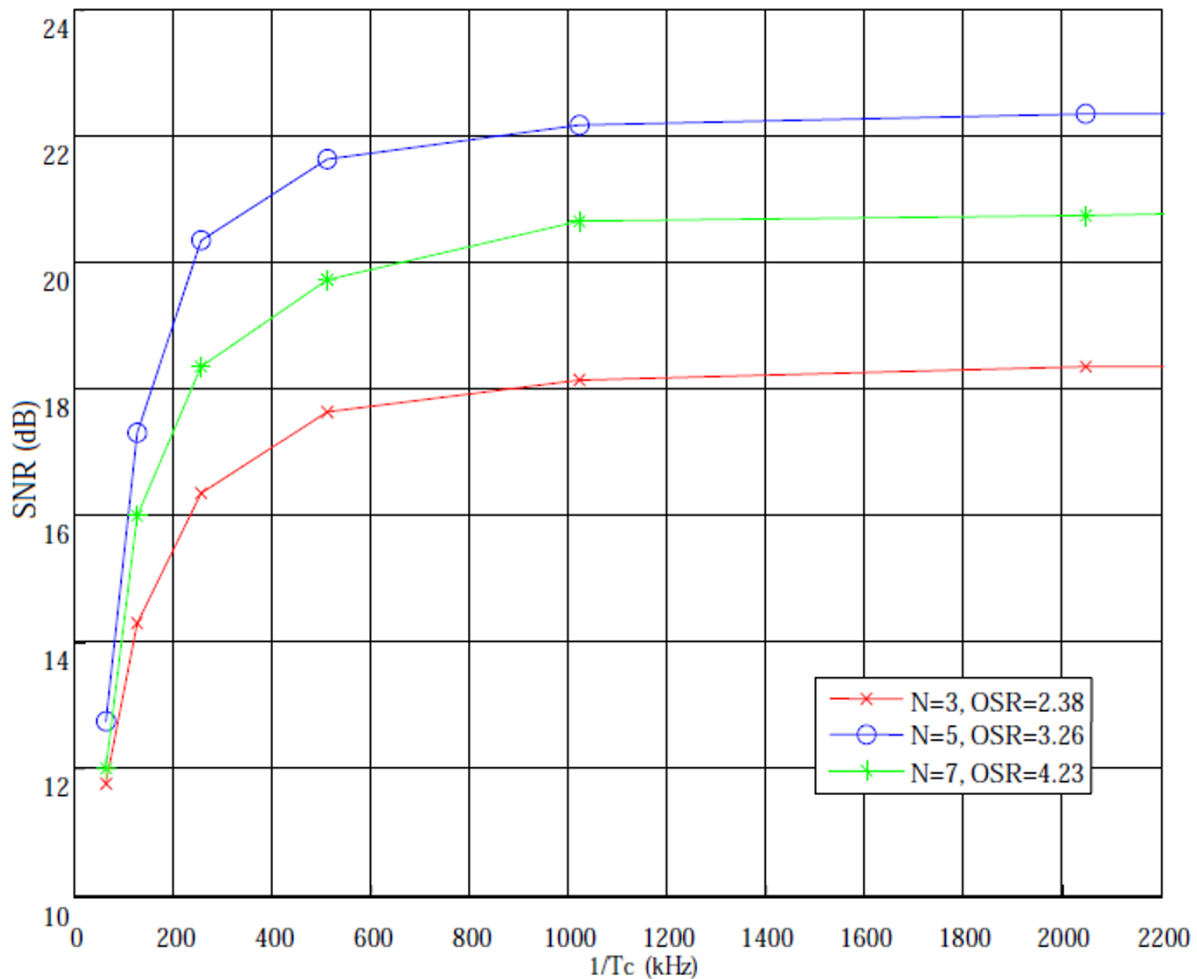


Figure 6 SNR versus precision of time quantizer ( $\frac{1}{T_c}$ ).

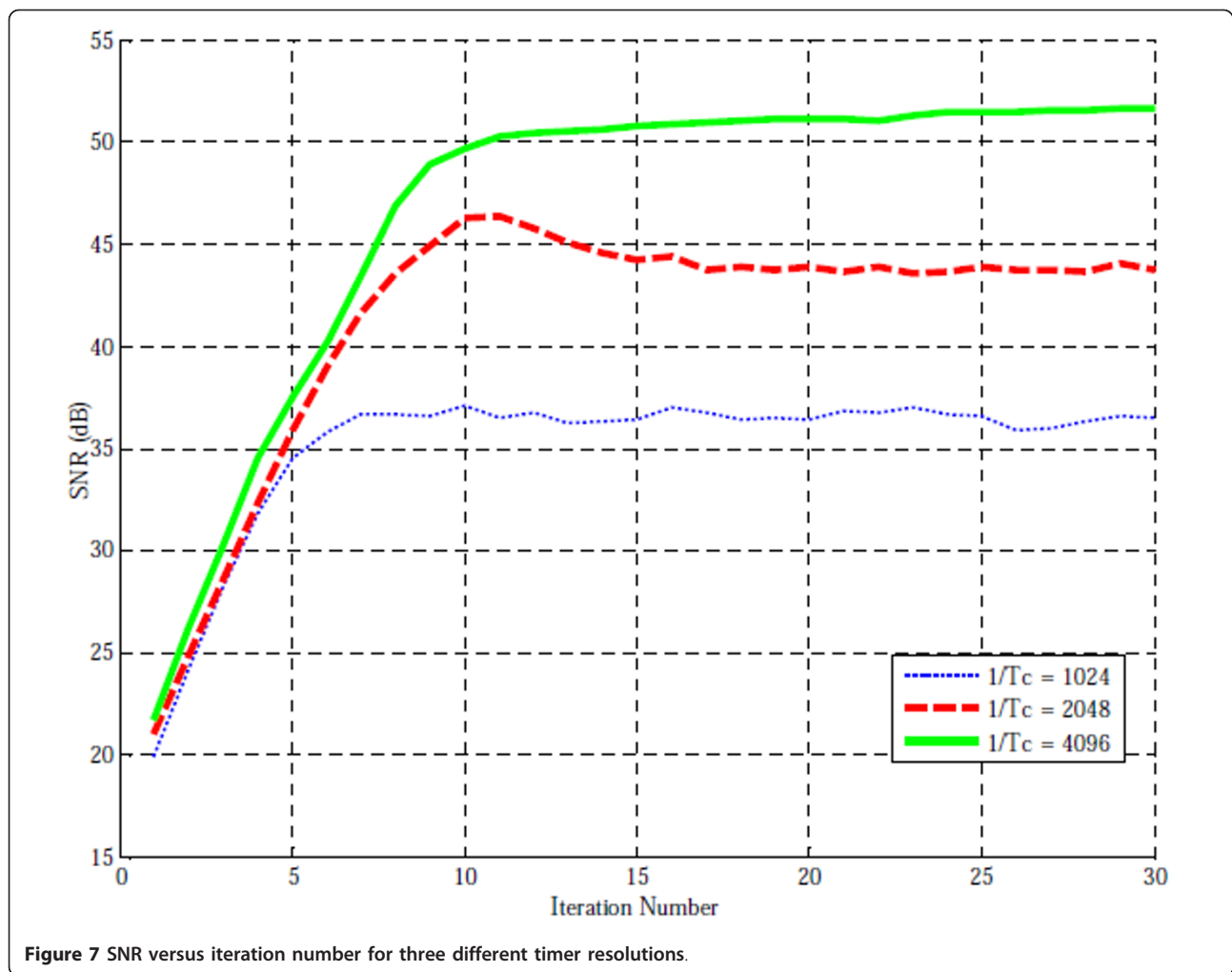
crossing sampler to uniform samples. Then, a decimator is used in order to reconstruct the original signal from interpolated samples in Nyquist rate. In a simple model for the asynchronous sigma-delta modulator, the error of level-crossing sampler is considered as an additive noise. Therefore, it can be realized that the error signal passes from a high-pass transfer function to receive in the output of the modulator and it causes noise shaping, which can improve performance of the system.

Table 1 Number of bits for reference levels versus precision of time quantizer ( $\frac{1}{T_c}$ )

Timer resolution (kHz)	OSR = 2.38	OSR = 4.23
64	6	5
128	7	6
256	8	7
512	9	8
1,024	10	9
2,056	11	10

The SNR of the reconstructed signal versus the precision of the time quantizer ( $\frac{1}{T_c}$ ) for different over sampling rates is shown in Figure 9. Similarly to Table 1, the number of bits that are needed to encode the difference time between samples for different timer resolutions ( $\frac{1}{T_c}$ ) is shown in Table 2. A comparison between Table 1 and Table 2 shows that maximum distance between samples in asynchronous SDMs is smaller than those in asynchronous DMs and it leads to a smaller number of bits for the time quantizer. The SNR versus the iteration number for three different timer resolutions is illustrated in Figure 10.

The total power consumption of the converter after a specific number of iterations ( $N$ ) can be obtained easily by multiplying the power of the one iteration by  $N$ . Dynamic power consumption is related to switch transitions and operating frequency of the circuit, while



static power consumption is directly related to the technology, which is used for the A/D converter implementation and should be measured after practical implementation of the converter [17]. Dynamic power consumption for our asynchronous converter can be obtained from the following equation:

$$P_{\text{dynamic}} = f_s \cdot C_{\text{Load}} \cdot (V_{dd})^2 + f_{clc} \cdot C'_{\text{Load}} \cdot (V_{dd})^2. \quad (15)$$

Where,  $C_{\text{Load}}$  and  $C'_{\text{Load}}$  are approximately in the range of (1-2) Picofarad and (100-200) Femtofarad, respectively. Also,  $f_s$  and  $f_{clc}$  are operating frequency of the circuit ( $\text{OSR} \cdot f_{\text{Nyquist}}$ ) and frequency of the timer clock, respectively. The right term of the above equation is the power, which is consumed by the timer clock. By comparing the operating frequency of the circuit in the synchronous and asynchronous converter with each other, it can be understand that asynchronous circuits are very effective converters in order to reduce dynamic power consumption.

A first-order asynchronous sigma-delta modulator is used in our simulation. Therefore, we compare its results with a first-order synchronous sigma-delta modulator. The number of quantization level for synchronous converters is considered equal to the number of reference levels in asynchronous one. The simulation results can be observed in Table 3. It can be found from this table that good enhancement in the converter can be achieved by using the level-crossing sampler instead of the amplitude quantizer in a sigma-delta converter. On the other hand, the complexity (simulation time  $T$ ) in an asynchronous converter is greater than that of an synchronous one. Also, it can be seen that, by increasing the timer resolution, the SNR of the reconstructed signal is increased and the SNR in the case that  $\frac{1}{T_C} = 8,192$  is about 7dB better than  $\frac{1}{T_C} = 4,096$  after 10 iterations.

Table 4 shows the sampling frequency, dynamic power consumption and Effective Number of Bits for different



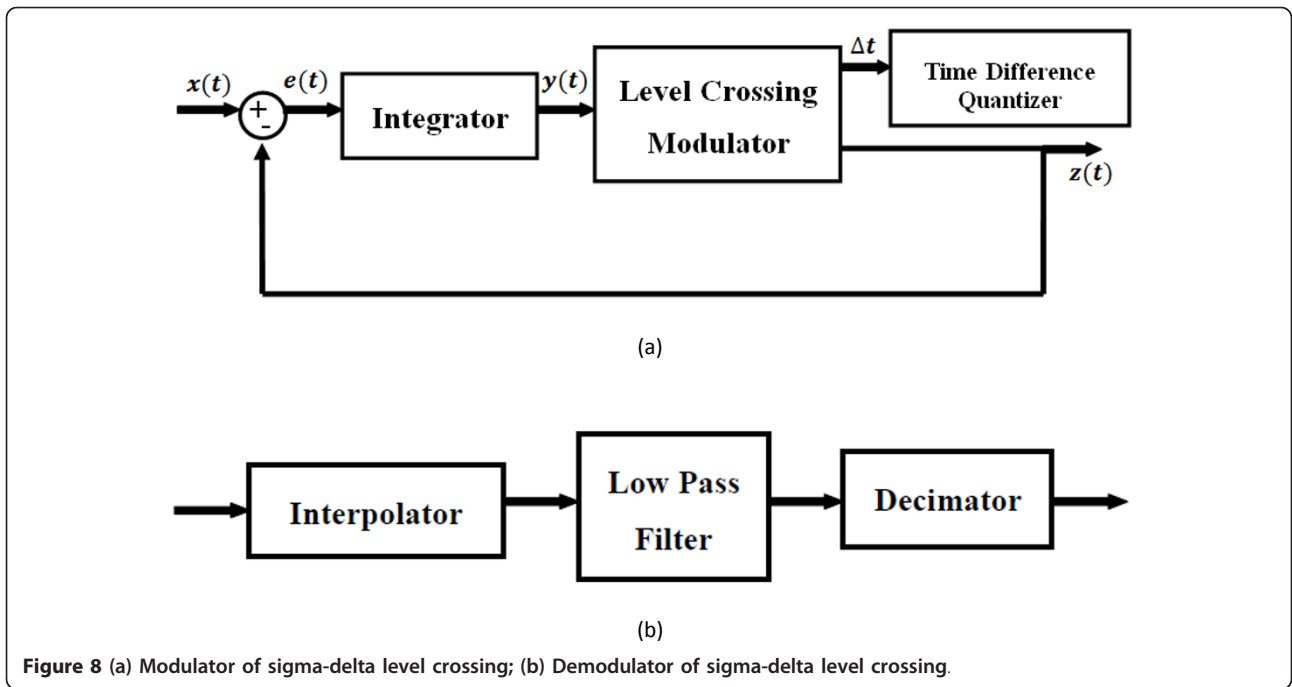


Figure 8 (a) Modulator of sigma-delta level crossing; (b) Demodulator of sigma-delta level crossing.

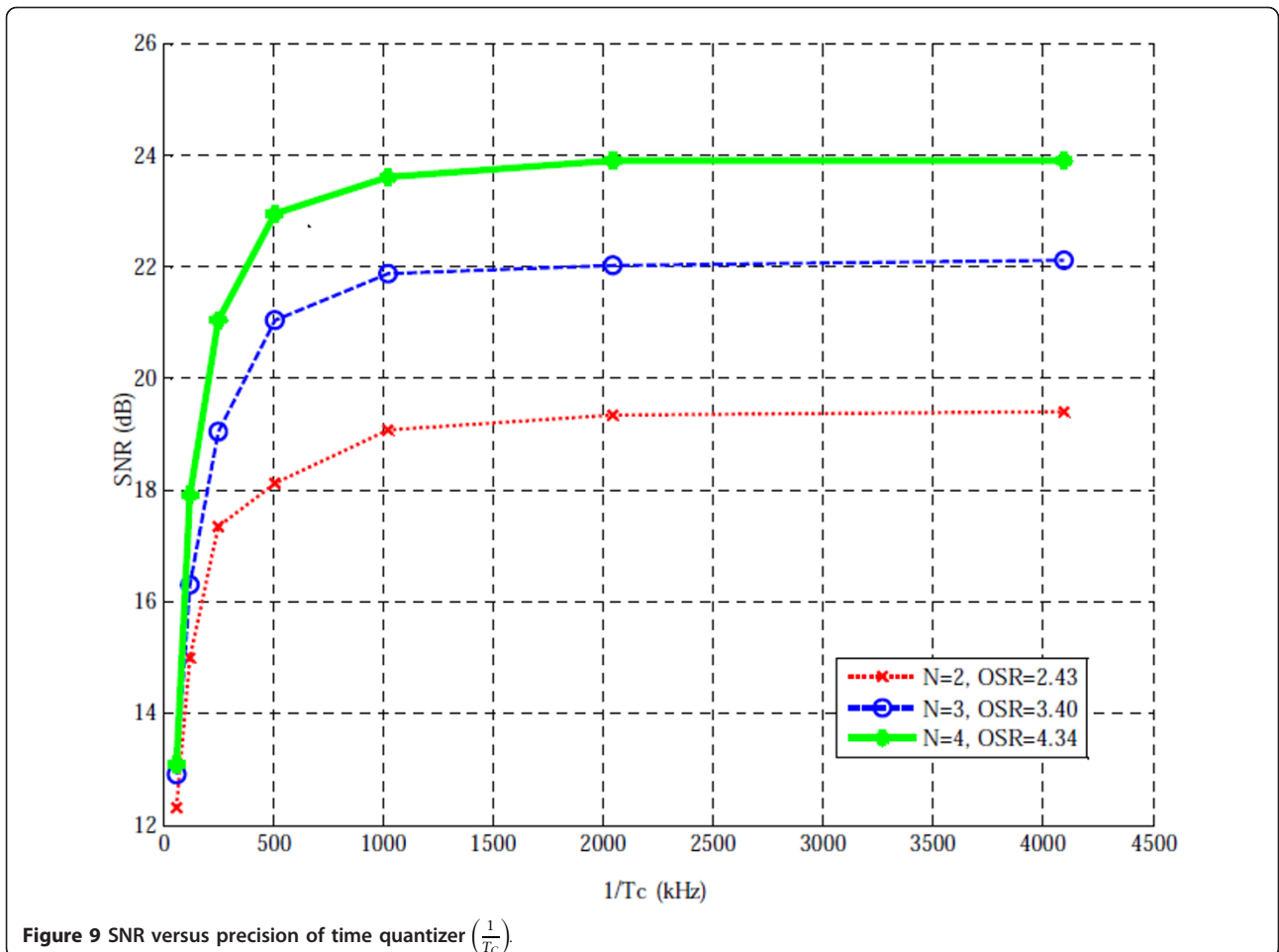


Figure 9 SNR versus precision of time quantizer  $(\frac{1}{T_c})$ .

**Table 2** Number of bits for reference levels versus precision of time quantizer ( $\frac{1}{T_c}$ )

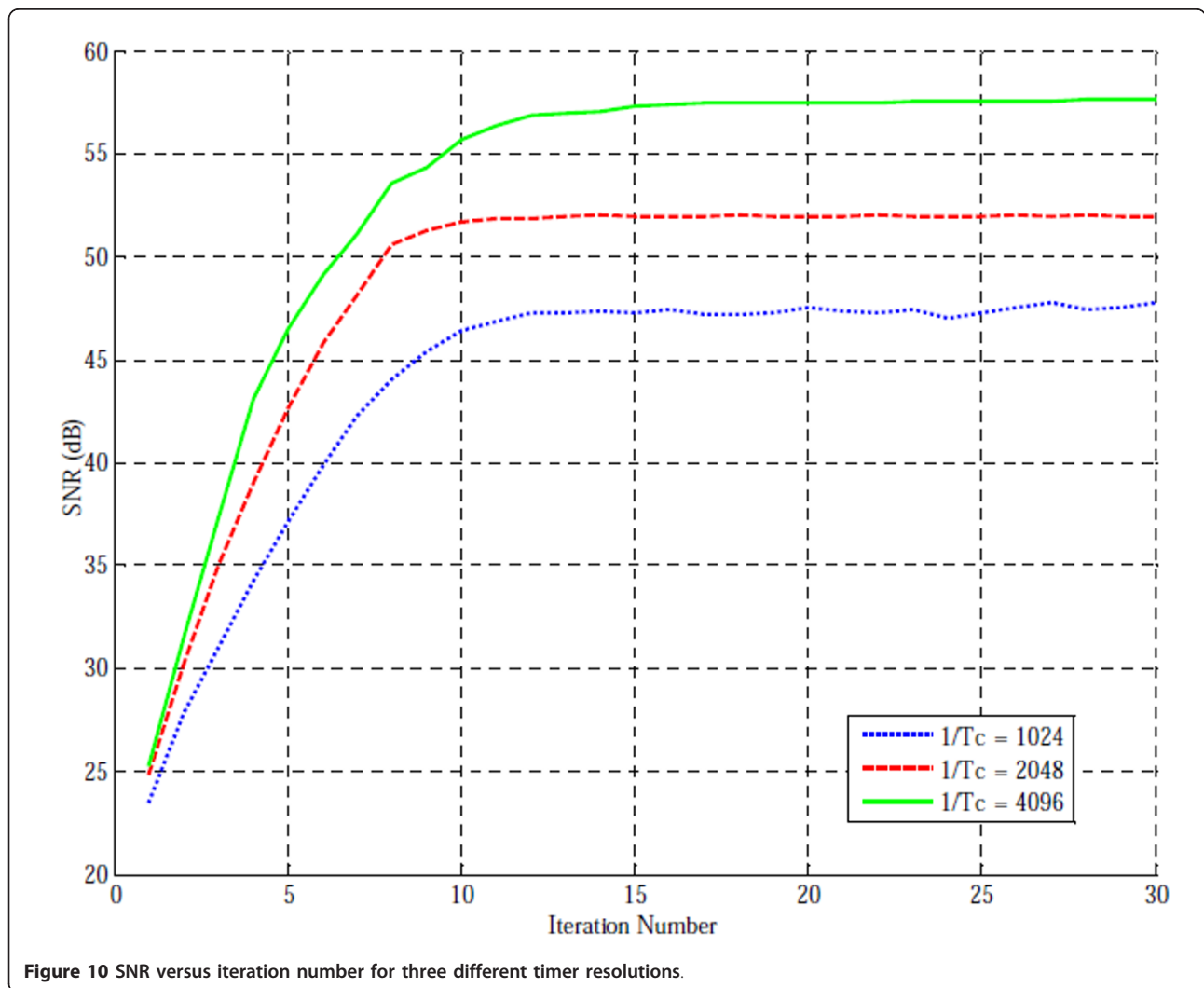
Timer resolution (kHz)	OSR = 2.43	OSR = 4.34
64	5	4
128	6	5
256	7	6
512	8	7
1,024	9	8
2,056	10	9

A/D converter. It can be found from this table that the resolution and dynamic power consumption of the asynchronous SDM converter after 10 iterations are more than other converters. However, one iteration of an asynchronous converter consumes less power than a synchronous converter.

### 5 Conclusion

This paper presents a new iterative algorithm to convert analog signal to digital (A/D) using an asynchronous A/D converter. In the proposed methods, converted samples are nonuniform, which decreases the number of additional samples and lead to decreasing in the power consumption. Simulation results demonstrate that the asynchronous sigma-delta modulator has better performance than the synchronous one, and its quality even can be enhanced by increasing the timer resolution.

The iterative algorithm is effective way to reconstruct original signal from the nonuniform samples of the asynchronous converter. Therefore, we use the iterative method to improve performance of these A/D converters and decrease the distortion caused by the SDM modulator. Hence, we can exploit filters with lower



**Figure 10** SNR versus iteration number for three different timer resolutions.

**Table 3 SNR of reconstructed signal for asynchronous and synchronous sigma-delta modulator for different iteration numbers**

Iteration number	Sigma-delta level crossing		Sigma-delta		
	OSR = 3.40		OSR = 16	OSR = 32	OSR = 64
	N = 3		N = 3	N = 3	N = 3
	$\frac{1}{T_c} = 4,096$ kHz	$\frac{1}{T_c} = 8,192$ kHz	T = 1.14 s	T = 1.23 s	T = 1.39 s
	T = 6.65s	T = 7.11s			
5	46.47	51.10	37.21	42.18	50.73
10	55.71	63.29	43.60	51.03	57.59
15	57.28	64.09	44.34	51.08	58.61
20	57.51	64.26	45.05	51.17	58.83
30	57.69	64.78	45.18	51.52	58.88

**Table 4 sampling frequency, dynamic power consumption and effective number of Bits for different A/D converter [18,19]**

A/D converter	Sampling frequency (KHz)	Timer frequency (KHz)	Effective number of bits (ENOB)	Dynamic power consumption ( $\mu$ W)
Folding converter	10,000	-	7.7	20
Pipeline converter	4,000	-	9.4	8
Delta level-crossing converter	34.72	4,096	7.35	8.8
(after 10 iterations)	34.72	8,192	8	17.1
Sigma-delta converter	512	-	8.2	5.12
(after 10 iterations)	1024	-	9.3	10.24
Sigma-delta level-crossing converter	27.2	4,096	9	8.73
(after 10 iterations)	27.2	8,192	10.2	16.92

degree in order to decrease the cost and complexity of the A/D converter.

These A/D converters have many applications because of their simple structure and low power consumption. Implementation of the iterative algorithm is simple, and it is unnecessary to change the configuration of the A/D converter in order to increase the number of iterations. Also, it must be mentioned that using the iterative algorithm to improve the performance of the system supports all types of SDMs with different orders and different numbers of quantization bits.

**Endnotes**

<sup>a</sup>Time Varying. <sup>b</sup>Compound Fourier Transform.

**Authors' contributions**

All authors participated in the preparation of the paper. MK developed the model and wrote the paper. Also, some part of the simulations are accomplished by MK. SB was involved in performing the simulations and verifying the results, and FM supervised all the work. All the authors contributed to the manuscript, and approved its final version.

**Competing interests**

The authors declare that they have no competing interests.

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