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An analysis of maximum likelihood estimation method for bit synchronization and decoding of GPS L1 C/A signals

Tiantong Ren* and Mark Petovello

Abstract

In weak GNSS signal environments, extending integration time is paramount to improving the GNSS receiver's sensitivity. Furthermore, sufficient coherent integration can help to mitigate multipath and cross-correlation false locks and avoid squaring loss. However, extending integration time is limited by the navigation message data bit, if present. The maximum likelihood (ML) estimation method has been shown as the most effective way to estimate the navigation bit boundary locations (i.e., bit synchronization) and subsequently estimate the data bit values (i.e., bit decoding) in the presence of noise alone. In this paper, the performance of ML bit synchronization and decoding is systematically assessed as a function of the number of data bits, the effect of Doppler error and received signal power in different tracking modes (i.e., phase-locked mode and frequency-locked mode). In addition, the theoretical performance models of ML bit synchronization and decoding are developed based on statistical theory. The experimental validation of the developed performance models and analyses is reported. For GPS L1 C/A signals, it is shown that for ML bit synchronization, using 100 data bits, the successful synchronization rate (SSR) can reach to about 100% with C/N_0 as low as 20 dB-Hz with no Doppler error. The performance degradation caused by Doppler error is not significant if the Doppler error is within 5 Hz, and with the maximum tolerance of 25 Hz, while for ML bit decoding, the successful decoding rate (SDR) of the 2-bit sequence can reach to about 100% with C/N_0 as low as 25 dB-Hz with no Doppler error. The performance degradation caused by Doppler error is not significant if the Doppler error is within 2 Hz. Both theoretical and simulation results establish that the upper bound of Doppler error for a 2-bit sequence is 12.5 Hz.

Keywords: GNSS (GPS) receiver; Standalone; Weak signal; High sensitivity; Extended integration; Bit synchronization; Bit decoding

1. Introduction

Global Navigation Satellite Systems (GNSSs) such as the Global Positioning System (GPS) can provide users with accurate navigation and timing services worldwide. They are vital for applications such as aircraft auto-piloting, automobile en-route guidance, pedestrian positioning, etc. Recently, processing weak GNSS signals has been receiving growing attention because of the increased demand for navigation indoors, under dense foliage canopies, and in urban canyons.

High-sensitivity GNSS (HSGNSS) receivers are capable of providing satellite measurements for signals attenuated by up to about 30 dB [1-3]. For HSGNSS receivers, extending integration time coherently is paramount to obtaining higher sensitivity, mitigating multipath and cross-correlation false locks, and avoiding squaring loss. However, longer coherent integration time is limited by the navigation message data bit, if present. For coherent integration beyond the data bit period, navigation data bit wipe-off is required to avoid energy loss that occurs due to bit transitions. Furthermore, complete bit wipe-off requires the knowledge of bit boundaries and bit values. The processes of determining the location of the bit boundaries and extracting the bit values are herein called bit synchronization and bit decoding, respectively.

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By using the navigation data bit aiding and frequency aiding from an external source, Akos et al. [4] showed that in acquisition stage signals with carrier-to-noise-density ratios (C/N_0) of 32, 22, 17, and 12 dB-Hz can be detected requiring coherent integration time of at least 8, 200, 400, and 800 ms, respectively. Similarly, the authors in [5-7]. used aiding information from wireless network broadcasting and Akopian and Syrjarinne [8] mentioned that network assistance can be used for bit synchronization by providing time and position information. However, all of these methods need access to external aiding sources, and the receiver will correspondingly lose its autonomy with a corresponding increase in complexity and cost.

Algorithms which do not require any external aiding source, e.g., histogram method [9], Viterbi algorithm [10], extended Kalman filter method [11], and maximum-likelihood (ML) algorithms [12,13], can determine the location of the data bit boundaries and the data bit values for a stand-alone GNSS receiver. Authors in [12,13] showed that the ML algorithms (i.e., ML bit synchronization and ML bit decoding) outperformed the other methods for weak GNSS signals.

The ML bit synchronization is first introduced in [12], and a brief assessment has showed that it outperforms the conventional histogram method in weak GNSS signal environments. However, all analyses in [12] were based on simulation results and no theoretical performance model had been developed. The ML bit decoding, introduced in [13] is reported to outperform other algorithms either in performance or complexity. However, the effect of different numbers of bits to be decoded at a time and the effect of Doppler error was not assessed in [13]. In [14], the requirements of ML bit synchronization and bit decoding algorithms were analyzed in terms of the number of data bits required for bit synchronization and the number of data bits that can be decoded at a time for bit decoding.

In the context of this work, the performance of bit synchronization and bit decoding is directly assessed in terms of the successful synchronization rate (SSR) with the navigation data bit (i.e., correct identification of the bit boundaries) and the successful decoding rate (SDR) of bit values. This contrasts with previous work [14], which focused primarily on fixed SSRs and SDRs. In addition, theoretical performance models are derived and experimentally validated. This paper also analyzes the effect of bit transitions for ML bit synchronization and the bound of frequency error for ML bit decoding in weak signals. Finally, the results are validated with multiple-trial test in a software-based GNSS receiver, and various implementation schemes are introduced and compared.

The contributions of this paper are three-fold. First, it systematically assesses the performance of ML bit synchronization and decoding as a function of the number of data bits, the effect of Doppler error and received signal power in phase-locked mode and frequency-locked mode by using Monte Carlo test. Second, it develops theoretical performance models of ML bit synchronization and decoding based on statistical theory. The performance models and analysis are experimentally validated. Third, it gives and compares different implementation schemes in a software-based GNSS receiver in weak signal environments.

One can consider these contributions to be important to current GNSS research because they provide answer to various queries such as follows: What kind performance can be expected from ML bit synchronization and decoding? What is the prerequisite for a stand-alone HSGNSS receiver to extend coherent integration based on the ML algorithms? How to configure a HSGNSS receiver design given a signal strength and Doppler frequency error level? What are the bounds of Doppler frequency error toleration? The answers to these questions are of great value for the designers of HSGNSS receivers.

The paper is organized as follows: Section 2 summarizes the ML estimation algorithms of bit boundaries and bit values. Section 3 gives the theoretical performance model of the ML estimation algorithms. Section 4 presents and analyzes the test results. The concluding remarks are given in Section 5.

The proposed algorithms are derived for a generic BPSK GNSS signal, but are assessed using GPS L1 C/A signals only. Although the methods presented do not apply to pilot signals (e.g., GPS L1C) due to the absence of data modulation (synchronizing with any possible secondary code is accomplished using very different techniques [15]), it is acknowledged that a pilot signal could assist with bit synchronization and decode for any data-bearing signal from the same satellite. This idea is beyond the scope of this paper.

2. Maximum likelihood estimation algorithms for bit synchronization and decoding

This section gives a brief overview of the ML algorithms for bit synchronization and decoding used in this paper.

2.1 Signal model

Consider a GNSS signal with the ratio (M) between data bit period (T_b) and ranging code period (T_c), that is $M = T_b/T_c$. In this case, the kth correlator output, computed over single code periods and sampled with $1/T_c$ Hz, of an N length of data sequence is given by [12]

$$R_k(\Delta\tau) = AG_k(\Delta\tau)b_{k,l_b} + n_k, \quad (k = 1, 2, ..., NM) \quad (1)$$

where $G_k(\Delta\tau)$ is the normalized ranging code correlation function, $\Delta\tau$ is the error in the locally generated ranging code, $A = |A|e^{j\Delta\varphi}$ is complex amplitude where $\Delta\varphi$ is the phase difference between incoming signal and locally generated carrier (this is approximately zero in phase-locked loop, in which case the amplitude degenerates to a real value), b_{k,l_b} is the navigation data bit value with transition at l_bth sample relative to the start of the current data bit. Assuming no error in the code phase estimation, i.e., $\Delta\tau = 0$, (1) can be rewritten as

$$R_k = Ab_{k,l_b} + n_k, \quad (k = 1, 2, ..., NM) \tag{2}$$

It is natural to have a small frequency error in the locally generated signal replica. To include the effect of Doppler errors, the signal model is updated as follows:

$$R_k(\Delta f_d) = |A| b_{k,l_b} \exp\{-j(2\pi\Delta f_d k T_c - \Delta\varphi)\} \operatorname{sinc}(\pi\Delta f_d T_c) + n_{I,Q}, \quad (k = 1, 2, ..., NM) \tag{3}$$

where Δf_d is the Doppler/frequency error, $n_{I,Q}$ is the complex form of additive white Gaussian noise and the *sinc* function represents the carrier spectrum.

2.2 ML bit synchronization

ML bit synchronization is the process of detecting bit boundary locations using a likelihood function. Since M is the ratio between data bit period and ranging code period, there are M possible bit locations. The likelihood function used is the sum of the absolute values of cross-correlation function between the prompt correlator output sequence and an MT_c ms window function. The concept behind ML bit synchronization is that every bit transition can contribute to detect the bit boundary, and more bit transitions at the same bit boundary can help to improve the SSR.

The ML bit synchronization algorithm in [12] is summarized below. The MT_c ms width window function is defined as

$$W_k = 1, (k = 1, 2, ..., M) \tag{4}$$

The matched filter output which is the cross-correlation between $R_k(\Delta f_d)$ in (3) and W_k is given by

$$C_{n,\bar{l}_b}(\Delta f_d) = \sum_{k=1}^{NM} R_k(\Delta f_d) W_{k-\left(nM+\bar{l}_b\right)}, \quad (n = 0, 1, ..., N-1) \tag{5}$$

where $\bar{l}_b$ is the initial edge shift of the window function in one bit period.

The ML estimate of the bit boundary locations can be found by selecting the location value that maximizes the sum (over time) of the absolute values of cross-correlation from the previous step. The sum of the absolute values of cross-correlation is given by

$$S_{\bar{l}_b}(\Delta f_d) = \frac{1}{N}\sum_{n=0}^{N-1} \left| C_{n,\bar{l}_b}(\Delta f_d) \right| \tag{6}$$

Then the ML estimate of bit boundaries is obtained as

$$\hat{l}_b = \underset{\bar{l}_b \in [1:M]}{\arg\max}\, S_{\bar{l}_b}(\Delta f_d) \tag{7}$$

2.3 ML bit decoding algorithm

Bit decoding is the process of determining bit values after the bit synchronization has been completed. The likelihood function used in the ML algorithm is the inner product between T_b ms prompt correlator outputs starting from a bit boundary (so as to avoid integrating over a boundary) and locally generated bit combinations. If trying to decode N bits at a time, the number of possible bit combinations is equal to 2^{N-1}, and the correct bit combination is supposed to have the maximum energy. It is noted that the energy based ML bit decoding method detects the bit transition instead of the actual bit values (i.e., there is a sign ambiguity), but this is sufficient for data wipe-off for extending integration time.

The ML bit decoding algorithm described in [13] is summarized here. The bit value combination matrix $\mathbf{B}$ $(2^{N-1} \times N)$ is defined as

$$\mathbf{B} = \begin{bmatrix} 1 & 1 & \dots & 1 \\ 1 & 1 & \dots & -1 \\ \dots & \dots & \dots & \dots \\ 1 & -1 & \dots & -1 \end{bmatrix} \tag{8}$$

For an N bit sequence, the inner product between $\mathbf{R_N}(\Delta f_d) = \left[R_{T_b,1}(\Delta f_d), R_{T_b,2}(\Delta f_d), ..., R_{T_b,N}(\Delta f_d)\right]$ (an N length vector containing the accumulated prompt correlator output (T_b ms)) and the vector $\mathbf{b_m}$ from the mth row of $\mathbf{B}$ is given by

$$I_m(\Delta f_d) = \mathbf{R_N}(\Delta f_d) \cdot \mathbf{b_m}, \left(m = 1, 2, ..., 2^{N-1}\right) \tag{9}$$

The ML estimate of bit values can be found by maximizing the energy of the inner product. The ML estimate of bit values is obtained as

$$\hat{\mathbf{b}} = \underset{\mathbf{b_m} \in [\pm 1 \pm 1 ... \pm 1]}{\arg\max} \left| I_m(\Delta f_d; \mathbf{b_m}) \right| \tag{10}$$

To summarize, the ML bit synchronization process is given by the following:

- Track the GNSS signals using either a phase-locked loop (PLL) or frequency lock loop (FLL);
- Perform correlations using T_c coherent integration intervals;

- Store a sequence of MN correlator output samples;
- Accumulate the correlator output samples coherently over the data bit interval, T_b, N times;
- Add the absolute of individual accumulations (this removes the need for a PLL);
- Shift the stored sequence of correlator outputs by one sample and repeat the above two steps; repeat this for all possible bit boundaries and identify the shift that yields the maximum output value.

3. Theoretical performance model

This section gives the theoretical performance models for bit synchronization and decoding.

Before looking at the mathematical details, it is noted that ML bit synchronization and decoding algorithms can work either in the phase-locked mode or in the frequency-locked mode. Generally, the tracking loop with carrier phase estimate (i.e., using a PLL) can provide more precise carrier phase and frequency estimates, but tracking only the carrier frequency using an FLL can tolerate higher user dynamics and frequency errors [16]. However, from Equation 3, the main impact of carrier tracking is the frequency error in the 'sinc' function, which only serves to attenuate the power passing through the tracking loop. In contrast, the phase error in the 'exp' term ultimately gets removed when the absolute correlator value is applied.

In addition, the ML bit synchronization and decoding processes require the pseudorandom noise (PRN) code being locked using a delay lock loop (DLL) such that the loss in signal power is negligible. To this end, a tracking error of better than 0.5 chips will lose a maximum of 6 dB. That said, the assumption of zero code tracking error (i.e., $\Delta\tau = 0$) in this paper makes the SSR independent from tracking methods and parameters. In other words, the results of SSR as a function of C/N_0 can be seen as the upper bound in real applications, and the worst case has 6 dB attenuation in power.

3.1 Theoretical performance model of ML bit synchronization

Consider the sum of the absolute values of cross-correlation in (6) when there is no Doppler error $\left(S_{\bar{l}_b} = S_{\bar{l}_b}(\Delta f_d = 0)\right)$, where Figure 1 shows $S_{\bar{l}_b}$ with the parameters of a GPS L1 C/A signal, that is T_b = 20 ms, T_c = 1 ms and M = 20. In this case, the bit transition location is set at the middle of a bit, that is 10 ms, and the T_c ms correlator outputs in (3) have been normalized. The probability of successful synchronization is given by

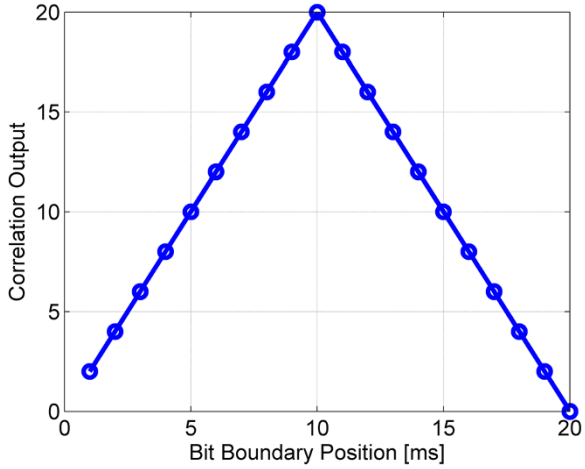

Figure 1 Cross-correlation output of one navigation data bit in ML bit synchronization.

$$\begin{aligned} P_s &= P\left(\bigcap_{\bar{l}_b=1,\bar{l}_b\neq l_b}^{M}\left\{S_{l_b} > S_{\bar{l}_b}\right\}\right) \\ &\approx P^2\left(\bigcap_{\Delta l_b=1}^{M/2}\left\{S_{l_b} > S_{l_b+\Delta l_b}\right\}\right) \end{aligned} \tag{11}$$

where $S_{\bar{l}_b}$ is the output at the bit boundaries, Δl_b is the difference between the estimated, $\bar{l}_b$, and the real, l_b, bit boundary location $\left(\bar{l}_b = l_b + \Delta l_b\right)$. A successful bit synchronization requires the output at the bit boundaries higher than any other outputs which are not at the bit boundaries. The probability of successful synchronization approximately equals to the square of one side probability of successful synchronization, which is the probability of S_{l_b} being higher than the left outputs or right outputs in Figure 1. It is approximate because the numbers of left outputs or right outputs are not necessarily equal, and this is the case when M is even, like GPS L1 C/A signals. A vector can be created containing the differences between the absolute value of cross-correlation at the bit boundaries and the non-bit boundaries as

$$\mathbf{X} = \begin{bmatrix} S_{l_b} - S_{l_b+1} \\ S_{l_b} - S_{l_b+2} \\ \cdots \\ S_{l_b} - S_{l_b+M/2} \end{bmatrix} \tag{12}$$

Then the probability of successful synchronization is given by

$$P_s \approx P^2(\mathbf{X} > \mathbf{0}) \tag{13}$$

The cross-correlation output in (5) is Gaussian distributed according to the signal model shown in (3). The sum of the absolute values of cross-correlation $S_{\bar{l}_b}$ is

nearly Gaussian distributed if the mean is large, the covariance is relatively small, and the number of bits is low. In this case, X can be approximately treated as a multivariate Gaussian. The mean of $S_{\bar{l}_b}$ is large when $\bar{l}_b \rightarrow l_b$ but close to zero when $\bar{l}_b \rightarrow l_b + M/2$. However, $S_{\bar{l}_b + M/2}$ has the least impact on $S_{\bar{l}_b}$, that is $\hat{l}_b$ least likely equals to $l_b + M/2$. So the approximation will not be significantly affected by the mean values, but will become less accurate with large covariance and increased number of bits because of the absolute operation in (7). However, if the number of bits increases continuously, i.e., $N \rightarrow \infty$, the approximation becomes accurate again because of the central limit theorem. The results shown later suggest that the above assumptions are indeed reasonable.

The probability density function of multivariate Gaussian distribution is mathematically expressed as follows:

$$f_{\mathbf{X}}(x_1, \ldots, x_{M/2}) = \frac{1}{(2\pi)^{M/4} |\sum|^{1/2}} \exp\left(-\frac{1}{2}(\mathbf{X}-\boldsymbol{\mu})^T \sum^{-1} (\mathbf{X}-\boldsymbol{\mu})\right) \tag{14}$$

where $\boldsymbol{\mu}$ is the mean vector and $\sum$ is the covariance matrix. With a normalized value of correlator output of T_c ms, the mean vector $\boldsymbol{\mu}$ and the covariance matrix $\sum$ can be given by

$$\boldsymbol{\mu} = \begin{bmatrix} 2 \\ 4 \\ \vdots \\ 2(M/2) \end{bmatrix} \tag{15}$$

$$\sum = \begin{bmatrix} 2 & 2 & \cdots & 2 & 2 \\ 2 & 4 & \cdots & 4 & 4 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 2 & 4 & \cdots & 2(M/2-1) & 2(M/2-1) \\ 2 & 4 & \cdots & 2(M/2-1) & 2(M/2) \end{bmatrix} \sigma^2 \tag{16}$$

where σ^2 is the variance of the T_c ms correlator outputs. Finally, the probability of successful synchronization in (13) can be written as

$$P_s \approx Q^2\left(\frac{\mathbf{0}-\boldsymbol{\mu}}{\sqrt{\sum}}\right) \approx Q^2\left(\frac{-\boldsymbol{\mu}}{\sqrt{\sum}}\right) \tag{17}$$

where $Q(\cdot)$ is the complementary cumulative distribution function [17,18].

In order to verify the theoretical performance model developed above, Monte Carlo (MC) simulations have been used to estimate the performance of ML bit synchronization quantified by SSR (i.e., the simulated probability of successful synchronization from tests). The simulation is based on the signal model given in (2), and includes a bit sequence in which the bit transition happens for every bit. The GPS L1 C/A signal parameters are used here and 10,000 trials were simulated for each C/N_0 value in Matlab™ platform. This is the setting for all the following MC simulations unless otherwise stated. It can be seen in Figure 2 that a good agreement between theoretical and simulation results can be achieved if the C/N_0 is higher than 20 dB-Hz, and the theoretical results are obtained based on (17). This establishes the validity of the developed theoretical performance model. The fact that the overall disagreement is small indicates that the Gaussian approximation made before is acceptable. When the C/N_0 is lower than 20 dB-Hz, the disagreement between the theoretical and simulation models increases with higher number of navigation data bits. This phenomenon is coincident with the earlier judgment. Furthermore, when the number of bits is continuously increased, the disagreement tends to decline at higher number of bits, e.g., 100 bits, because of the central limit theorem as discussed before. The relationship among the SSR, the number of bits and the number of bit transitions will be discussed in the following section.

Generally, longer coherent integration time periods such as 2 s (100 bits) would have concerns about oscillator stability and code Doppler. However, the ML bit synchronization process with a high number of bits such as 100 bits only sums the correlator output samples coherently to the length of the window function in (4) (i.e., the length of 1 bit, which equals to 20 ms for GPS L1-C/A signals), followed by non-coherent accumulation to 2 s. Therefore, the oscillator stability and code Doppler will not have obvious impact on ML bit synchronization.

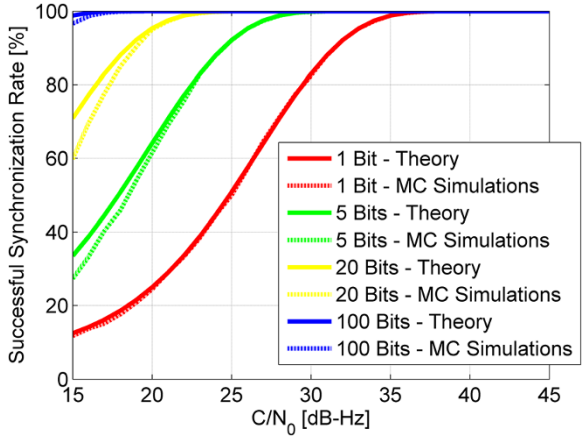

Figure 2 Theoretical and simulated performance of ML bit synchronization as a function of signal strength. Different numbers of navigation data bits are considered. Ten thousand trials were simulated for each C/N_0 value.

3.2 Theoretical performance model of ML bit decoding

The bit error rate (BER) of coherent decoding (e.g., from PLL) for BPSK signal is given by [17,18]

$$P_{e,\mathrm{coh}} = Q\left(\sqrt{\frac{2E_b}{N_0}}\right) = Q\left(\sqrt{2\cdot 10^{0.1\cdot C/N_0}\cdot T_{\mathrm{co}}}\right) \tag{18}$$

where E_b is the transmitted signal energy per bit, N_0 is a specified noise spectral density, and T_{co} is the coherent integration time and set as the bit length here. The probability of successful decoding in phase-locked mode is given by

$$P_{d,\mathrm{PL}} = \left(1-P_{e,\mathrm{coh}}\right)^N \tag{19}$$

The above expression indicates that if the probability of successful decoding for a single bit is used as a criterion, the performance of ML bit decoding in phase-locked mode is insensitive to the number of bits to be decoded at a time.

The BER of non-coherent decoding (i.e., differential decoding, e.g., from FLL) for BPSK signal is given by [17,18]

$$P_{e,\mathrm{diff}} = \frac{1}{2}\exp\left(-\frac{E_b}{N_0}\right) = \frac{1}{2}\exp\left(-10^{0.1\cdot C/N_0}\cdot T_{\mathrm{co}}\right) \tag{20}$$

Given the above, the probability of successful decoding for two bits to be decoded at a time in frequency-locked mode is given by

$$P_{d,\mathrm{FL},N=2} = \left(1-P_{e,\mathrm{diff}}\right) \tag{21}$$

A precise theoretical performance model for more than two bits to be decoded at a time has not been developed yet. However, assuming that the performance of ML bit decoding in frequency locked mode is insensitive to the number of bits to be decoded at a time (later we will confirm with a multiple-trial test), an approximate form can be given based on (21) as

$$P_{d,\mathrm{FL}} \approx \left(1-P_{e,\mathrm{diff}}\right)^{\frac{N}{2}} \tag{22}$$

Equations 19, 21, and 22 represent the first known relationship between the probability of successful decoding and the BER and are collectively one of the main contributions of this work.

MC simulations are used to estimate the performance of ML bit decoding quantified by SDR (i.e., the simulated probability of successful decoding from tests). The simulation is based on the signal model given in (2) and (3). As shown in Figures 3 and 4, a good agreement between the theoretical results of (19) and (21) and the simulation results has been found, suggesting the validity of the theoretical performance model. The approximate result of (22) also fits the MC simulation curves, although discrepancies are present. This means that the performance of ML bit decoding in frequency-locked mode is nearly insensitive to the number of bits being decoded.

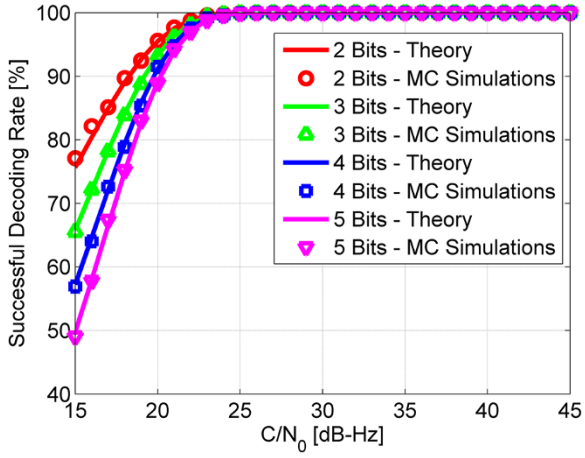

Figure 3 Theoretical and simulated performance of ML bit decoding in the phase-locked mode. Different numbers of navigation data bits are considered.

4. Test results and analysis

In this section, simulation results assessing the performance of ML bit synchronization and decoding under different conditions are reported. Monte Carlo simulations have been performed to estimate the performance curve.

Furthermore, all algorithms have been assessed in a software-based GNSS receiver platform called GSNRx™, which is developed in C++ by the PLAN group,

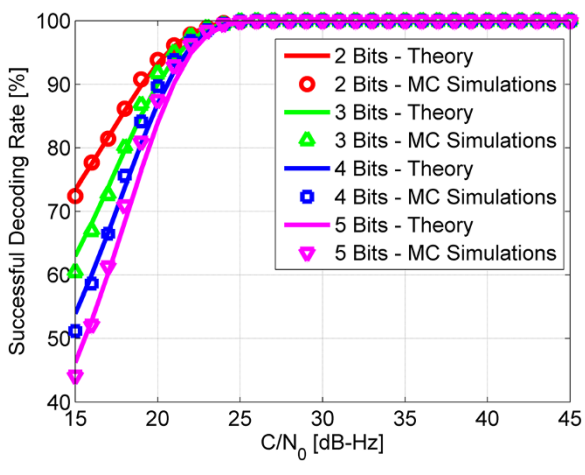

Figure 4 Theoretical and simulated performance of ML bit decoding in the frequency-locked mode. Different numbers of navigation data bits are considered.

University of Calgary. A dataset with various signal power levels were generated using a Spirent GS7700 GNSS simulator. Approximately 1 h of data was collected using a National Instruments PXI-5600 front-end (Austin, TX, USA) which includes an oven-controlled crystal oscillator (OCXO). The front-end parameters are shown in Table 1.

4.1 Performance of ML bit synchronization

4.1.1 Number of bits vs. number of bit transitions

The simulation results in Figure 2 show that the performance of ML bit synchronization improves with higher number of bits used. This is true only when the actual number of transitions increases as the number of bits considered increases. However, to assess performance for different scenarios, three kinds of bit sequences are implemented and tested: first, a bit transition is present at every bit; second, a bit transition is present every 2 bits; third, bit transitions occur randomly with a probability equal to 50%. Note that in the first case, a minimum of 2 bits need to be considered; similarly, a minimum of 4 bits need to be considered for the second case. The last test is a good emulation of real GNSS messages, and the number of bits considered will normally be greater than two (herein we consider a minimum of four).

Considering ML bit synchronization in phase-locked mode, Figure 5 shows that the performance of the first and the second kind of bit sequence are nearly similar. The reason is because both sequences have the same number of bit transitions even though they use a different number of bits. This result confirms the former assumption that generally the performance of ML bit synchronization is determined by the number of bit transitions and not the absolute number of bits. The reason bit transitions are significant is because without them, the result in Equation 6 will be approximately constant for all possible shifts considered, to within the level of the noise. In other words, without any bit transitions, the decision of the bit synchronization process would be based solely on noise. In Figure 5, a disagreement can be noticed between the solid line (when the bit transition happens every 2 bits) and the dashed line (when the bit transition happens every bit) when C/N_0 is low. This confirms that using longer bit sequences containing no bit transitions can degrade bit synchronization performance when C/N_0 is low.

Table 1 Front-end parameters used for collecting GNSS data

Parameter	Value (MHz)
Center frequency	1,575.0
Sampling rate	3.0
Bandwidth	2.5

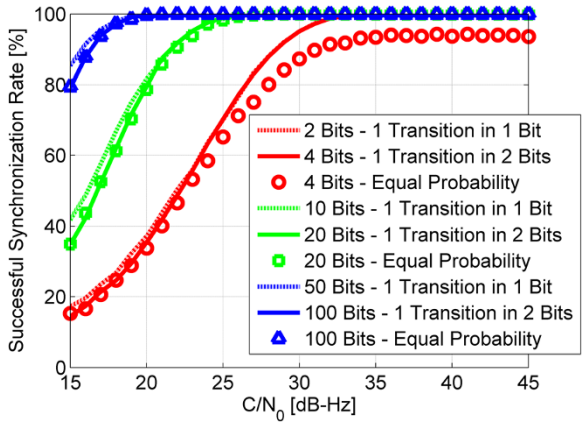

Figure 5 Simulated performance of ML bit synchronization as a function of signal strength. Different numbers of navigation data bits with different kinds of bit sequences are considered.

Without a priori knowledge about navigation message, the bit values/transitions in real GNSS data cannot be predicted. This coincides with the third kind of bit sequence. Figure 5 also shows the results between the second and the third kind of bit sequence are almost similar if the number of bits is larger than 20. The following simulations will only use the third kind of bit sequence unless otherwise stated. A separation between the theoretical model and the simulation result when the number of bits is low (e.g., red lines/dots in Figure 5) is observed. This is due to a lack of the bit transitions when the number of bits is low.

4.1.2 Comparison in phase-locked mode and frequency-locked mode

The performance results related to ML bit synchronization discussed in the preceding subsection are based on the phase-locked mode. This subsection presents a comparison between the phase-locked and the frequency-locked mode.

Figure 6 summarizes the results of the simulation and Spirent GNSS data processing. As can be seen, a small degradation in the frequency-locked mode can be viewed with the simulation data. This matches with the analysis made in Section 3.2.

Moreover, the results from the software-based GNSS receiver GSNRx™ are also shown in Figure 6. A test with thousands of trials has been performed in the receiver by intentionally restarting the bit synchronization process (without a priori information) every time a bit synchronization result is obtained (regardless of the outcome). With the coherent integration time of 1 ms, the receiver in the Kalman filter tracking mode [19] can track the signal power to 28 dB-Hz in a static scenario.

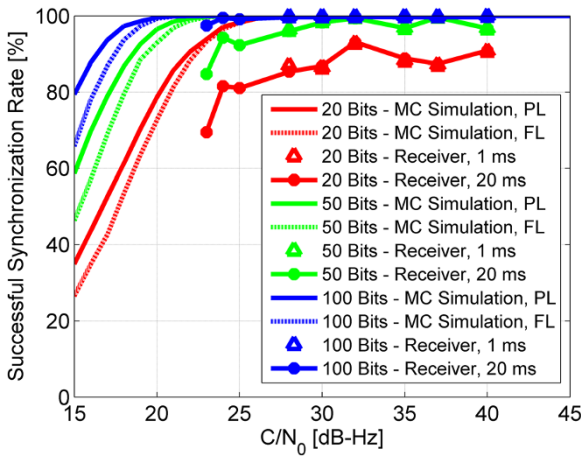

Figure 6 Simulated and real performance of ML bit synchronization as a function of signal strength. Different numbers of navigation data bits are considered in phase-locked mode and frequency-locked mode.

With the coherent integration of 20 ms, the receiver of the same mode can track the signal power to 23 dB-Hz. In addition, the coherent integration of 20 ms can have a better estimation of Doppler, as shown in Figure 7.

These results indicate the necessity of extending coherent integration time. Without knowledge of bit boundaries, it is impossible to extend coherent integration time to 20 ms, and the result is only for assessing the performance of ML bit synchronization in low C/N_0 environment. However, the tracking threshold can be extended by advanced tracking methods, e.g., vector tracking, Doppler aiding, and ultra-tight integration with inertial sensors. This paper does not consider these methods but shows the performance of ML bit synchronization lower than 28 dB-Hz. For the receiver

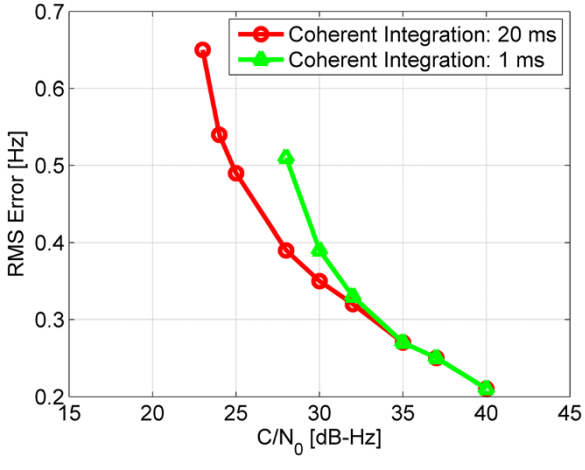

Figure 7 RMS errors of Doppler estimation as a function of signal strength. Two different coherent integration times are considered.

results, the trend seems coincident with the former conclusion that a higher number of bits results in better performance. However, the receiver results appear a bit worse than the simulation results. This is because in real navigation data message, there would be a higher possibility for some words (e.g., reserved words) containing unchanging data bit. The ML bit synchronization might totally fail without any bit transition. It can be seen in Figure 8 that the plus ones last longer than 3 s in the data set. This causes the ML bit synchronization with 100 bits to fail once and those with 20 bits to fail seven times even without noise.

Based on the results discussed above, there are three recommended schemes for implementing the ML bit synchronizer in a GNSS receiver. First, choose different numbers of bits for synchronization according to current signal power and the possible Doppler errors (the effect of Doppler errors will be introduced later). This scheme is efficient to achieve bit synchronization, but the tradeoff is that it is vulnerable to the bit sequence without bit transitions. A method detecting if bit transitions existed was reported in [12] by a hypothesis testing. The bit boundary will be declared if the ratio between the cross-correlation output from the candidate of the boundary position (maximum value) and the output from the candidate shifted by 10 ms (supposed minimum value) passes a certain threshold. Second, choose a relatively large number of bits for synchronization no matter the values of signal power and other parameters. This scheme is the easiest to be implemented but is less efficient and requires longer time for bit synchronization. Third, choose the number of bits either according to current parameters (e.g., estimated C/N_0) or fixed as one trial, but do not declare the position of the bit boundaries unless the certain number of continuously successful trials is achieved. This scheme can increase the reliability of synchronization results but also increase the system complexity as a tradeoff.

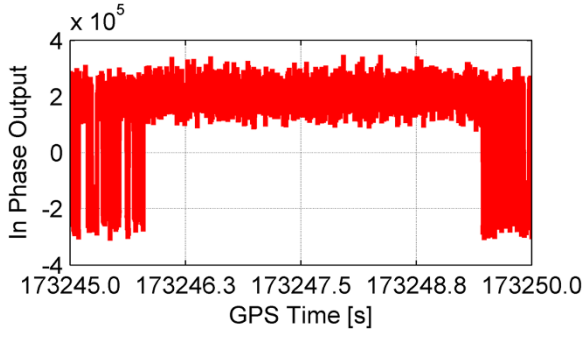

Figure 8 In phase correlator output in phase-locked mode.

4.1.3 Effect of Doppler errors

Any Doppler tracking errors may contaminate the synchronization performance. The simulation results of 20 and 100 bits with the Doppler error from 0 to 26 Hz are shown in Figures 9 and 10. Three phenomena can be viewed: first, the increased Doppler errors degrade the synchronization performance; second, the performance degradations are not significant if the Doppler error is within 5 Hz; third, the SSR decreases rapidly if the Doppler error is equal or higher than 25 Hz. The third phenomenon happens because the bit synchronizer cannot distinguish a real bit transition and a reversal caused by frequency errors if the error is equal or higher than 25 Hz.

4.2 Performance of ML bit decoding

The performance of ML bit decoding being assessed in this paper assumes that successful bit synchronization has been achieved.

4.2.1 Comparison in phase-locked mode and frequency-locked mode

The same conclusion that the performance of ML bit decoding is insensitive and nearly insensitive to how many bits to be decoded at a time in coherent and noncoherent decoding, respectively, is further pursued in this section. With the case of two bits to be decoded at a time, a comparison between the results from the simulation and the receiver in the phase-locked mode and the frequency-locked mode is shown in Figure 11. The results from the receiver fit the MC simulation curves though a small discrepancy can be noticed at about 23 dB-Hz. This is due to the fact that the receiver loses lock around 23 dB-Hz, and the insufficient samples may result in the biased results in the multiple-trial test. To illustrate, 100,000 trials were run for every C/N_0, and the results were generated from all 50 min of valid outcomes (i.e., data bit period) for $C/N_0 \geq 25$ dB-Hz, but from only a few seconds of valid outcomes for C/N_0 around 23 dB-Hz because of lost lock.

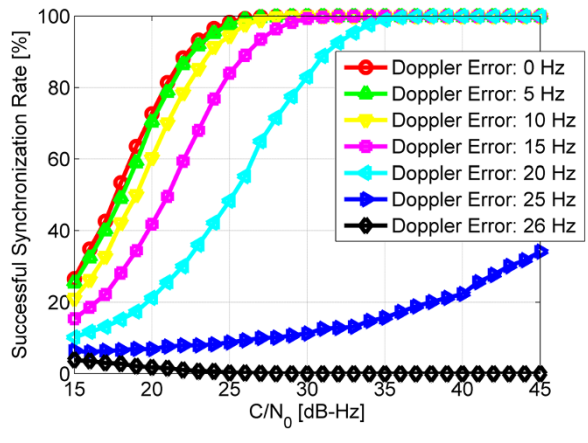

Figure 9 Simulated performance of ML bit synchronization with 20 bits. Different Doppler errors are considered.

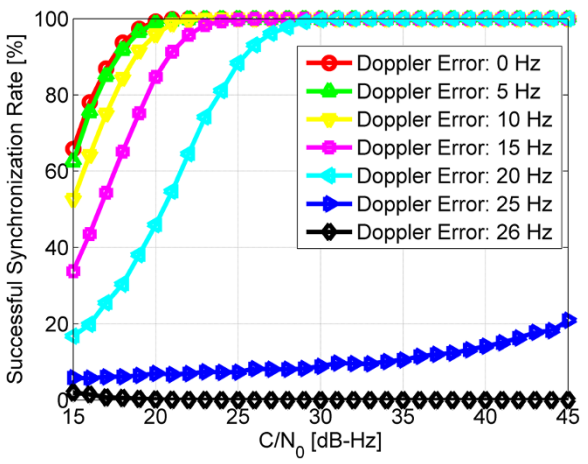

Figure 10 Simulated performance of ML bit synchronization with 100 bits. Different Doppler errors are considered.

4.2.2 Effect of Doppler errors

The existence of the Doppler errors contaminates the bit decoding performance. Consider the case of two bits to be decoded at a time. In this case, the inner product between the T_b ms prompt correlator output vector and the possible bit value vector $\mathrm{b_m}$ in (9) is given by

$$\begin{aligned} I_m(\Delta f_d) &= \mathbf{R_N}(\Delta f_d)\cdot\mathbf{b_m}, \quad (m=1,2) \\ &= \sum_{k=1}^{2}\left(R_{T_b,k}(\Delta f_d)\bar{b}_{m,k}\right), \quad (m=1,2) \end{aligned} \tag{23}$$

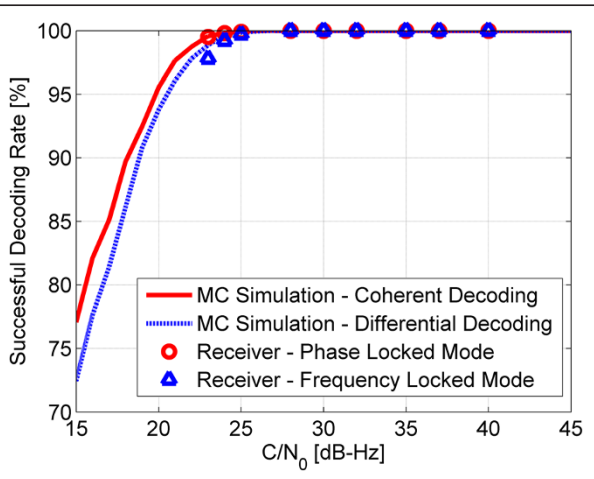

Figure 11 Simulated and real performance of ML bit decoding as a function of signal strength. Two bits to be decoded at a time are considered in phase-locked mode and frequency-locked mode.

where $N = 2$, Δf_d is the Doppler error, and $\bar{b}_{m,k}$ is the kth element in vector $\mathbf{b_m}$. Substituting (3) into (23) and omitting noise gives

$$I_m(\Delta f_d) = \sum_{k=1}^{2} \left(A_{T_b} b_k \exp\{-j(2\pi\Delta f_d k T_b + \Delta\varphi)\} \times \mathrm{sinc}(\pi\Delta f_d T_b) + n_{I,Q} \right) \bar{b}_{m,k} \quad (24)$$

where A_{T_b} is the amplitude of T_b ms correlator output. Except for the noise, one can also omit the irrelevant initial phase difference $\Delta\phi$ and the sinc function. Then a simplified result is obtained as

$$I_m(\Delta f_d) \approx A_{T_b} \exp\{-j2\pi\Delta f_d T_b\} \times \left(b_1 \bar{b}_{m,1} + b_2 \bar{b}_{m,2} \exp\{-j2\pi\Delta f_d T_b\} \right) \quad (25)$$

and the ML bit decoding result in (10) is only affected by $\left(b_1 \bar{b}_{m,1} + b_2 \bar{b}_{m,2} \exp\{-j2\pi\Delta f_d T_b\} \right)$. For comparison, for the case without Doppler error, the corresponding equation is $\left(b_1 \bar{b}_{m,1} + b_2 \bar{b}_{m,2} \right)$. Correspondingly, the Doppler error can make the process fail if

$$2\pi\Delta f_d T_b \geq \pi/2 \quad \Delta f_d \geq 1/(4T_b) \quad (26)$$

The reason Doppler errors contaminate the bit decoding performance is that the likelihood function $|I_m(\Delta f_d; \mathbf{b_m})|$ in (10) is determined by the magnitude of the sum of two vectors - $b_1 \bar{b}_{m,1}$ and $b_2 \bar{b}_{m,2} \exp\{-j2\pi\Delta f_d T_b\}$ - and any phase error ($2\pi\Delta f_d T_b$) in the second vector will reduce the tolerance of noise. More specifically, when the phase error is equal or larger than $\pi/2$, the magnitude resulting from the incorrect bit sequence will be equal or greater than the magnitude obtained with the true bit sequence even without noise, and this will result in a totally failed test. So without considering the effect of the noise, the upper bound of Doppler error for ML bit decoding with a 2-bit sequence for the GPS L1 C/A signal is 12.5 Hz ($T_b = 20$ ms). Of course, receiver noise will make the transition between frequency errors greater or smaller than 12.5 Hz more gradual.

The simulation result of ML bit decoding with a 2-bit sequence is shown in Figure 12. Four phenomena can be observed: first, the increased Doppler errors degrade the bit decoding performance; second, the performance degradations are not significant if the Doppler error is within 2 Hz; third, the SDRs increase with C/N_0 if the Doppler error is equal or less than 12 Hz; fourth, the SDR is about 50% if the Doppler error is equal to 12.5 Hz, meaning that the value of the likelihood function in (10) is the same whether a bit transition exists or not; fifth, the SDR decreases rapidly with increasing C/N_0 if the Doppler error is larger than 12.5 Hz. This result obtained validates the theory developed above. It confirms that the upper bound of Doppler error with a 2-bit sequence is 12.5 Hz.

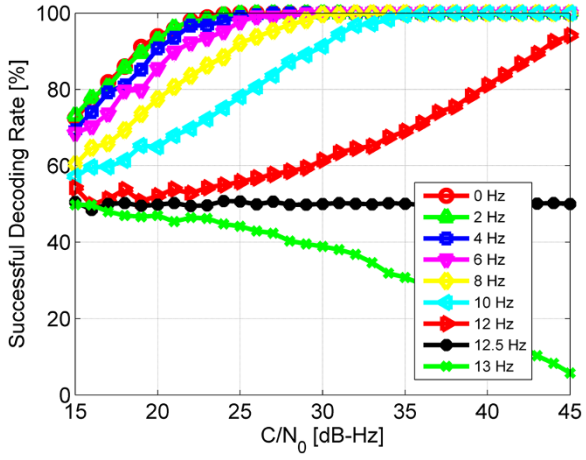

Figure 12 Simulated performance of ML bit decoding with a 2-bit sequence. Different Doppler errors are considered.

For the sake of comparison, the simulation result of ML bit decoding with a 5-bit sequence is shown in Figure 13. The SDR is very low (around 20%) when C/N_0 increases if the Doppler error is equal to 5 Hz. This indicates the tolerance of Doppler error with a 5-bit sequence (about 4 Hz) is much lower than a two bits sequence (12.5 Hz).

The results above show that the performance of ML bit decoding is insensitive/nearly insensitive to how many bits to be decoded at a time. This is true if there is no Doppler error. However, based on the analysis above, the bit sequence with more bits to be decoded at a time has lower ability to tolerate Doppler error. So the

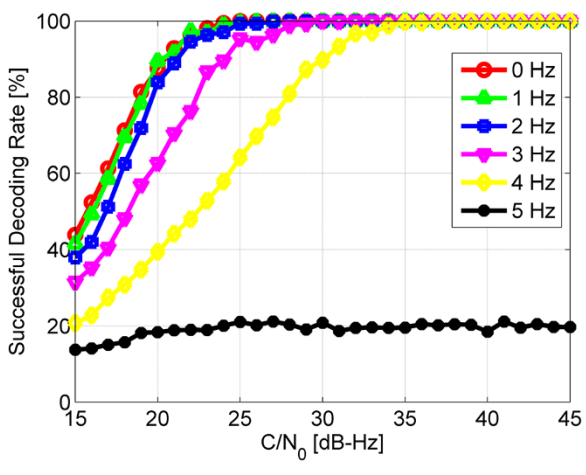

Figure 13 Simulated performance of ML bit decoding with a 5-bit sequence. Different Doppler errors are considered.

configuration with a 2-bit sequence (the minimum number of bits in ML bit decoding) is the optimum scheme.

The Doppler errors also have a destructive effect in the signal acquisition (searching) stage. However, the cause of the effect for ML bit synchronization and decoding is different. In the acquisition stage, the standard 2/3 T_{co} (i.e., coherent integration time) or 1/2 T_{co} Doppler offset rules are usually used to determine the size of search bins in Doppler domain in order to avoid large attenuation due to Doppler errors (via the sinc function). The effects of Doppler error in this paper will degrade and even invalidate the ML bit synchronization and decoding process, and the phase error is an accumulation of Doppler errors.

5. Conclusion

This paper presents a systematic analysis of the performance of ML bit synchronization and decoding. The performance is estimated as a function of the number of data bits, the effect of Doppler error and received signal power in the context of stand-alone GNSS receivers containing different tracking modes (i.e., phase-locked mode and frequency-locked mode). In addition, the theoretical performance models of ML bit synchronization and decoding are developed based on statistical theory. These models are being reported for the first time. The performance models and analysis have been experimentally validated. Finally, this paper presents the comparison of different implementing schemes in a software-based GNSS receiver in weak signal environments.

Generally the performance of ML bit synchronization is determined by the number of bit transitions, not the absolute number of bits. For the most common case that bit transition happens with a probability equal to 50%, a higher SSR, a lower C/N_0 and a higher Doppler frequency error all require more data bits. For GPS L1 C/A signals, by using 100 data bits, the SSR can reach to about 100% with C/N_0 as low as 20 dB-Hz with no Doppler error. The performance degradation caused by Doppler error is not significant if the Doppler error is within 5 Hz. The maximum tolerance of Doppler error is 25 Hz.

Without Doppler error the performance of ML bit decoding is insensitive/nearly insensitive to how many bits are being decoded at a time in phase-locked mode and frequency-locked mode, respectively. The bit sequence with more bits to be decoded at a time has lower ability to tolerate Doppler error. So, in the presence of Doppler errors, the optimum configuration is the 2-bit sequence, which is the minimum number of bits available in ML bit decoding. For GPS L1 C/A signals, the SDR of the two bits sequence can reach to about 100% with C/N_0 as low as 25 dB-Hz with no Doppler error. The performance degradation caused by Doppler error is not significant if the Doppler error is within 2 Hz. Both theoretical and simulation results show that the upper bound of Doppler error for a 2-bit sequence is 12.5 Hz.

Future work will use more field tests under different environments to confirm the results presented here. Also, the information will be used to define parameters within a software receiver in order to improve navigation performance.

Competing interests

The authors declare that they have no competing interests.

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