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A PAM4 transceiver design scheme with threshold adaptive and tap adaptive

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Abstract

To meet the demand of low bit error rate and high bandwidth for high-speed links, a reliable 112 Gb/s four-level pulse amplitude modulation (PAM4) transceiver design scheme with adaptive threshold voltage and adaptive decision feedback equalizer is proposed in this paper. In this scheme, three continuous time linear equalizers (CTLEs) at the front end of receiver are used to compensate the high-frequency, mid-frequency and low-frequency signals, respectively, and the variable gain amplifier (VGA) and saturation amplifier (SatAmp) are used to scale the signal amplitude. In addition to the three data samplers, four auxiliary samplers are also used for threshold adaptation. The sign-sign least mean squares algorithm uses the offset between the data sampler and the auxiliary sampler at the receiver side to drive the auxiliary reference voltage to converge to the signal constellation level, thus ensuring that the eye diagram of the PAM4 received signal has equal spacing and a constant signal–noise ratio for the three eyes in the vertical direction. In addition, the adaptive DFE for PAM4 signaling allows the transceiver to better adapt to the channel and thus achieve better equalizer performance. The simulation results show that the PAM4 transceiver design can compensate up to 25 dB of channel loss with an average eye height of 59.6 mv and an average eye width of 0.27 UI at a bit error rate of 10^{-12} under the condition of 3-tap feedforward equalizer (FFE) transmitter.

Keywords: Decision feedback equalization, Pulse amplitude modulation 4, Transceiver design, Self-adaption algorithm

1 Introduction

With the advent of technologies such as machine learning and artificial intelligence that require high data throughput, data processing needs in data network centers have grown exponentially. The increasing bandwidth demands of data centers and high-performance computing systems require higher I/O data rates per lane, driving the development of electrical interface standards that utilize PAM4 [1]. Among them, the international standards organization Optical Internetworking Forum (OIF) has released version 5.0 of the Common Electrical I/O Working Protocol IA which defines PAM4 signaling at 112Gbps [2].

Compared to not-return-to-zero (NRZ), PAM4 signals with half the Nyquist frequency have higher spectral efficiency, which is an attractive solution for high-speed

links with severely bandwidth-constrained channels. However, the use of PAM4 modulation technology also brings great challenges to the design of transceivers [3]. In general, transmitters designed for PAM4 signaling must be able to provide higher swings because the corresponding receivers need to efficiently resolve smaller amplitudes compared to NRZ signaling. Furthermore, the transmitter must maintain good linearity when transmitting the four PAM4 levels. The direct current (DC) level distortion caused by the nonlinearity of the transmitter will reduce the effective eye height seen by the receiver [4]. At the receiving end, the PAM4 receiver is more sensitive to noise and residual inter-symbol interference (ISI) under the limits of the transmit swing. Therefore, in order to minimize residual ISI, more tapped transmitter FFE and receiver DFE are required [5, 6]. While analog-to-digital converter (ADC)-based solutions offer greater flexibility in the number of equalizer taps, the power consumption and clock and data recovery (CDR) loop delays are prohibitive [7].

The objective of this paper is to improve the quality of the eye diagram and reduce the BER of the signal by reducing the design complexity of the equalizer under the joint action of the transmitter and receiver. Ultimately, the result will be an improvement in the overall performance of the system. Therefore, a high-performance PAM4 transceiver design scheme is proposed in this paper in order to avoid the complexity caused by ADC schemes. The overall architecture of the proposed transceiver is shown in Fig. 1. A 3-tap FFE is introduced in the transmitter to pre-emphasize the input signal, and an analog front end with three-stage CTLE and VGA, CDR and 4-tap DFE is involved in the half-rate receiver [8–12]. For DFE design simplification, the architecture of direct feedback is adopted, and the semi-interleaved feedback method is proposed to further improve the feedback speed under the condition of satisfying key timing constraints [13]. Sampler threshold adaptive operation is introduced to address sampling errors caused by reduced eye height in the PAM4 signal [14]. At the same time, the adaptive adjustment of the DFE taps further enhances the ability of the transceiver to adapt to the channel [15].

The basic principles of the 112 Gb/s PAM4 transceiver design are introduced in Sect. 1. Section 2 focuses on the proposed 4-tap semi-interleaved feedback DFE architecture and the design of the overall architecture of the PAM4 receiver using this DFE. Section 3 presents the proposed DFE threshold adaptation scheme and separately illustrates the different situations that arise during the adaptation process. Then, the tap adaptation algorithm of the 4-tap half-rate DFE architecture proposed

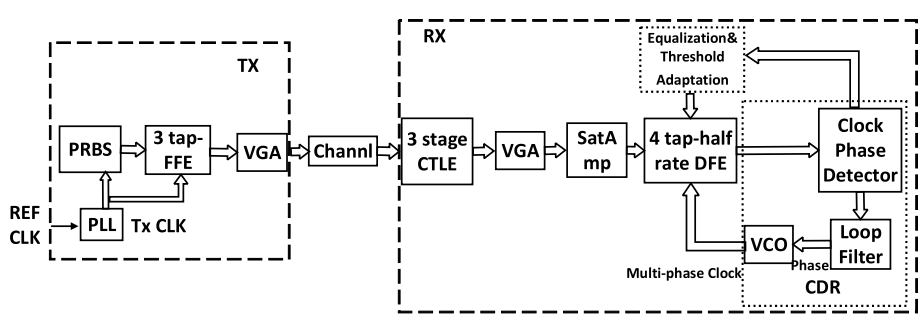

Fig. 1 Overall block diagram of the transceiver

in this paper is introduced. In Sect. 4, simulation is performed for the proposed transceiver and the research results are presented. Section 5 gives the conclusion.

2 DFE and receiver overall architecture design

2.1 4-tap half-rate half-interleaved direct feedback DFE

At data rate of tens or even hundreds of gigabits per second, equalization is essential for channel losses elimination. Linear equalizers such as FFE can effectively cancel ISI in channels with smooth loss profiles, but not as effective as in channels with spectral notches resulting from reflections due to connectors and via stubs. This motivates the use of nonlinear DFEs in receivers to overcome these drawbacks. Extensive research into DFEs has yielded a multitude of architectures, which can be broadly classified into "direct" or "unrolled" (speculative) DFEs with "full-rate" or "half-rate" clocks [16].

DFE stands out among equalizers for its significant advantage of being able to cancel post-pulse ISI without introducing noise and cross talk. However, the feedback timing path is challenging. In a full-rate direct feedback DFE implementation as shown in Fig. 2, the symbol decision and delay through the feedback finite impulse response filter logic must be done within one symbol or unit interval. This is often difficult to implement at high data rates due to the uneven distribution of logic delays among delay elements causing critical feedback timing paths to be significantly longer than iteration boundaries [17]. The loop unrolling technique involves precomputing all possible equilibrium values before a decision is actually fed back. These precomputed possible equalization values are then sliced to obtain all possible decisions for the input symbols. Finally, the multiplexer selects the correct decision by using past feedback decisions. However, this way of reducing critical path delays introduces exponentially increased complexity, especially in PAM4 systems.

The proposed DFE architecture is optimized basing on the combination of half-rate and direct feedback to reduce the complexity of the DFE design and simplify the CDR design. The detailed structure of the DFE is shown in Fig. 3. The feedback loop of the half-rate DFE structure is divided into odd and even channel where two opposing clock signals turn the input signal into two half-rate output signals. In order to further reduce the summing node load while reducing power consumption and design complexity, a direct feedback method is adopted. There are 4 feedback paths each for odd and even

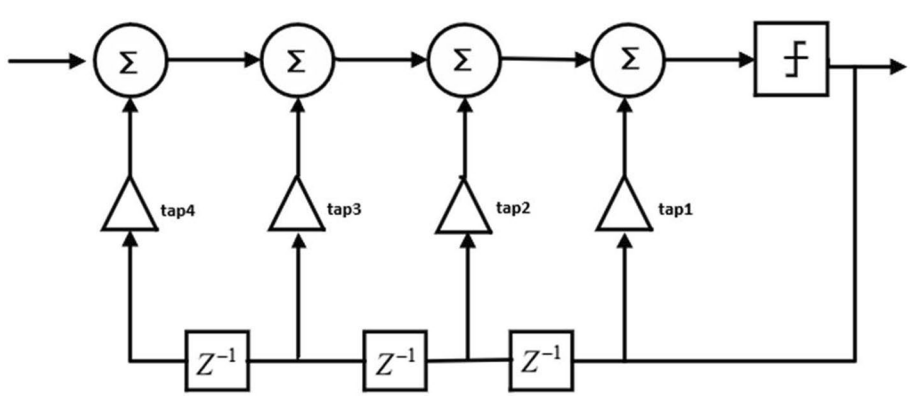

Fig. 2 Full rate 4-tap direct feedback DFE

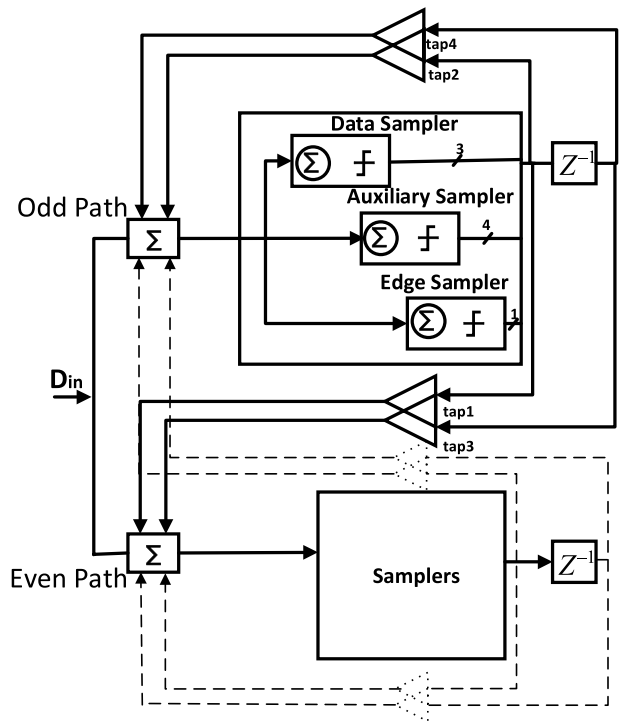

Fig. 3 4-tap half-rate half-interleaved direct feedback DFE detailed block diagram

channel in this DFE. For the odd channel, the signal in the tap 1 path is sent to the adder of the even channel as a feedback signal after passing through the sampler. In the tap 3 path, the signal passes through the delay unit after the sampling output and is then fed back to the adder of the even channel. The signals in the tap 2 path and tap 4 path undergo the same sampling and delaying process as tap 1 and tap 3, respectively, but the feedback signals in these two paths will be sent to the odd channel. This half-interleaved feedback method has two advantages over the conventional feedback method shown in Fig. 4, in which all four taps are completely interleaved. On the one hand, only half of the signal is fed back to the other branch, which greatly decreases the number of delay units used, which means that the complexity and power consumption of the DFE design are reduced. On the other hand, the DFE feedback path timing must satisfy the condition of less than one unit interval time, and the optimization of the DFE structure makes the critical path timing constraints less stringent. In the odd and even channel, the feedback time of the branch where the first two taps are located remains unchanged, and the feedback time of the other branches is shortened, which promotes the feedback speed.

2.2 DFE sampler design

A reliable PAM4 receiver requires not only equalization settings, but also a robust configuration of boost sampler thresholds. Figure 5 illustrates the data, auxiliary and edge sampler naming conventions and ideal sampling locations and sampler critical phase clock paths for PAM4 signals in this paper. During each sampling unit interval (UI), three data samplers (DH, DZ and DL) are used to detect the PAM4 signal. Among them, the threshold value of the sampler in the middle is set to 0, and the threshold value of

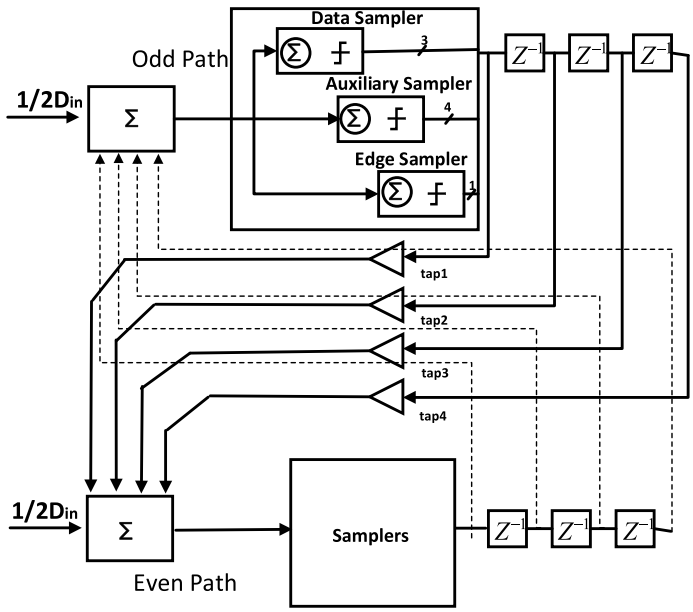

Fig. 4 4-tap half-rate fully interleaved direct feedback DFE detailed block diagram

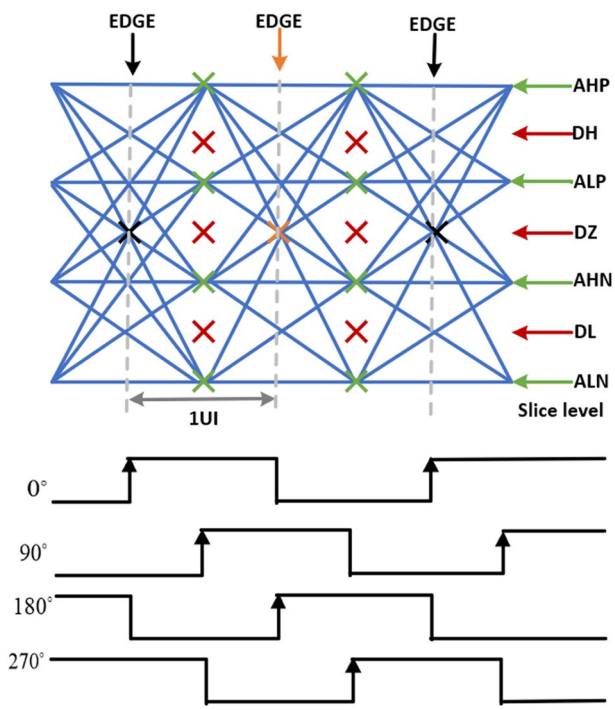

Fig. 5 PAM4 data sampler, auxiliary sampler and edge sampler names and sampler clock phase

the upper and lower samplers is set to $\pm 2/3$ of the amplitude of the equalized signal received by the threshold value adaptation circuit. Four auxiliary samplers (AHP, ALP, AHN and ALN) are used to provide reference information for the threshold voltage and tap adaptation of the data sampler. In the proposed DFE architecture, there are a total of four half-rate phase clocks in the odd and even channels for data, auxiliary and

edge detection, where auxiliary samplers and three data samplers are driven by the same phase clock, and the edge samplers in each path use a separate phase clock.

2.3 The overall architecture of the receiver

The overall architecture of the proposed PAM4 receiver is shown in Fig. 6. The RX analog front end (AFE) is composed of three-stage CTLE, VGA and SatAmp. Under the premise of the minimum channel working margin specified by IEEE 802.3ck specification for 112G, 3-stage CTLE for different frequencies is designed. The first-stage CTLE is mainly used to boost high-frequency signals to compensate for signal loss near the Nyquist frequency, with a DC gain of − 20 dB and a peak gain of up to 17 dB. The second-stage CTLE is designed to compensate for loss at middle frequency to eliminate the long tail of ISI. The DC and peak gains are − 6 dB and 0 dB, respectively. The peak frequency is constant at 10 GHz. The third-stage CTLE has constant DC gain (0 dB). The RX-side analog signal that has been partially equalized by the AFE is sent to a half-rate 4-tap DFE module which implements PAM4 data, auxiliary and edge sampling and DFE summing operations on the mixed signal. Three data samplers are used to detect PAM4 symbols, and an auxiliary sampler is added to each of the four PAM4 levels to ensure the stability of the data sampler threshold voltage. A bang-bang clock phase detector is used to determine whether an edge is sampled early or late. The sampling information of auxiliary samplers and data samplers is adaptive to tap and threshold voltage under the action of adaptive algorithm.

3 DFE threshold and tap adaptive design

PAM4 receiver sampler thresholds and equalization settings need to be changed accordingly as channel conditions variation [18, 19]. Performing adaptive operations on sampler thresholds and taps can be beneficial for more complex channel environments. This section describes sampler threshold voltage adaptation and DFE tap adaptation schemes with four auxiliary samplers.

3.1 Threshold adaptation

The nonlinearity at the transmitter and receiver is usually compressible, which results in reduced eye margins for the three eyes in the PAM4 eye diagram. This requires certain measures to improve the accuracy of eye threshold placement. Threshold adaptation is

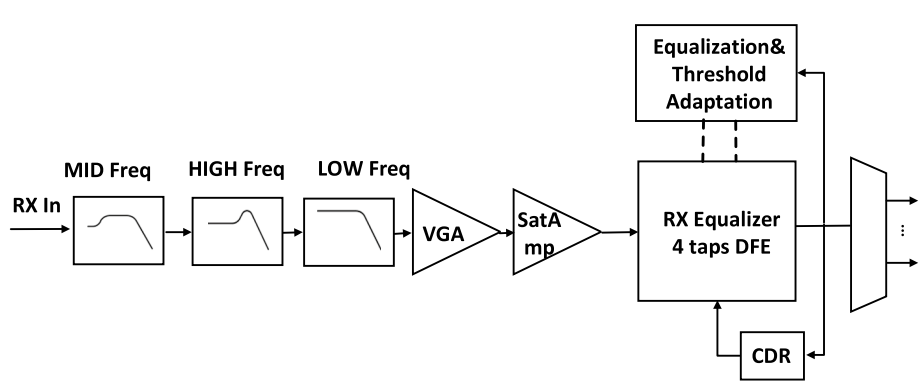

Fig. 6 Overall architecture of the receiver side

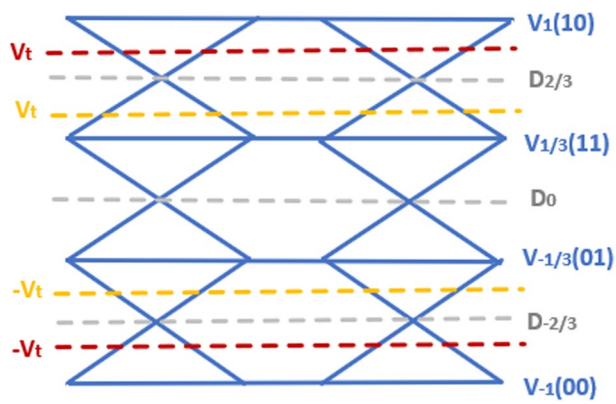

Fig. 7 The two states of the average of the adjacent levels of the auxiliary sampler

implemented according to the offset between the auxiliary sampler and the data sampler. Conceptually, the auxiliary samplers will return the same number of logic highs and lows on average when their reference voltages converge to the signal constellation value. At this point, the estimated level average between adjacent signal constellation voltages is then derived as the data sampler threshold. If the auxiliary reference voltage differs significantly from the signal constellation value, the mean value of the sampler output will deviate, and this relative offset is used by the sign-sign least mean squares algorithm to drive the auxiliary reference voltage to converge to the signal constellation voltage.

Here, we denote the four voltages of the signal constellation level as V_1, $V_{1/3}$, $V_{-1/3}$ and V_{-1}, representing 10, 11, 01 and 00, respectively. Where $V_1 = -V_{-1} = 3V_{1/3} = -3V_{-1/3}$, the ideal three data threshold voltages are $D_{2/3}$,D_0 and $D_{-2/3}$. The differences between adjacent levels are equal, so the final $D_{2/3}$ and $D_{-2/3}$ should be twice as large as $V_{1/3}$ and $V_{-1/3}$, respectively. According to the naming rules for samplers in the previous section, the voltages sampled by the four auxiliary samplers (AHP, ALP, AHN and ALN) are recorded as AUX_1, $AUX_{1/3}$, $AUX_{-1/3}$ and AUX_{-1}, respectively. The average values of adjacent sampled voltages are denoted as V_t, 0 and $-V_t$, respectively.

During the adaptive process, the auxiliary sampler gradually converges to the signal constellation level according to the reference voltage obtained by sampling. When the sampling voltage AUX_1 of the auxiliary sampler AHP is greater than $D_{2/3}$ ($AUX_1 > D_{2/3}$), the data received by decoding are regarded as $+1$, and the grayscale is mapped to 10. If the sampling voltage of the auxiliary sampler ALP is $0 < AUX_{1/3} D_{2/3}$, the decoded received data are regarded as $+1/3$, and the grayscale is mapped to 11. When the sampling voltage of the auxiliary sampler AHN is $D_{-2/3} < AUX_{-1/3} < 0$, the data received by decoding are regarded as $-1/3$, and the grayscale mapping is 01. When the sampling voltage AUX_{-1} of the auxiliary sampler ALN is less than $D_{-2/3}$ ($AUX_{-1} < D_{-2/3}$), the data received by decoding are regarded as -1, and the grayscale mapping is 00. If the average value of the adjacent levels of the auxiliary sampler is close to the ideal three data threshold voltages and the ratio of the returned logic 0 and 1 is close to 1:1, the sampler is considered to be sampling at the correct position.

As shown in Fig. 7, where the red dashed line indicates that the average adjacent level of the auxiliary sampler is greater than the ideal data threshold voltage, and the yellow dashed line indicates that the average adjacent level of the auxiliary sampler is

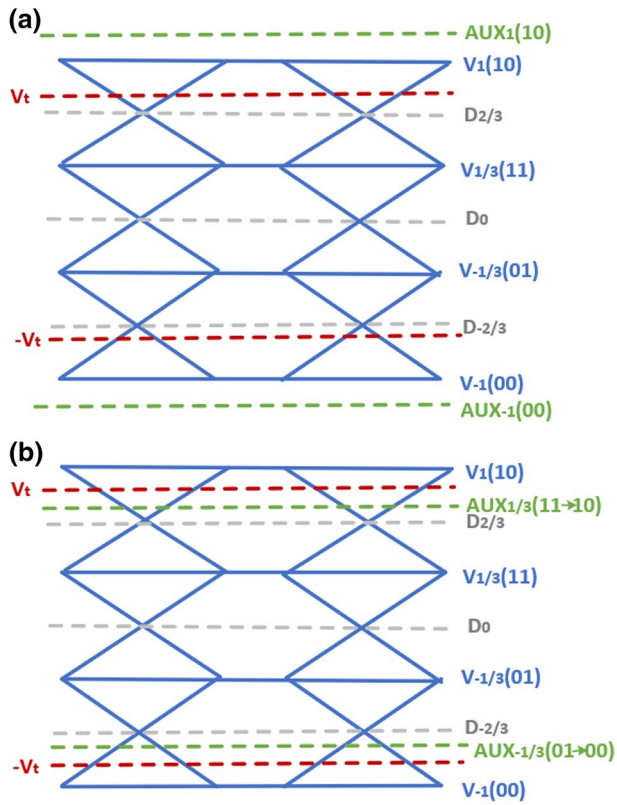

Fig. 8 AHP and ALN sampling results **a** large (red, green) and **b** small (yellow, black)

less than the ideal data threshold voltage. If $V_t > D_{2/3}$ and $-V_t < D_{-2/3}$ as shown by the red dashed line, then two cases can be derived at this point, the sampling results of the auxiliary samplers AHP and ALN are too large, or the sampling results of ALP and AHN are too large. Further analysis shows that the values of $|AUX_1|$ and $|AUX_{-1}|$ will to be decreased if the ratio of zeros and ones returned is still 1:1 and the sampling results and average values at this situation are shown in Fig. 8a. If the proportion of zeros and ones is not equal and the proportion of zeros is close to 75%, then the situation shown in Fig. 8b is met, and $|AUX_{1/3}|$ and $|AUX_{-1/3}|$ will be decreased. As shown by the yellow dotted line in Fig. 7, if $V_t < D_{2/3}$ and $-V_t > D_{-2/3}$, it can be concluded that the sampling values of AHP and ALN or ALP and AHN are small as shown in Fig. 9a or Fig. 9b. If the percentage of zeros and ones returned is not equal and the percentage of ones reaches 75%, it conforms to the situation shown in Fig. 9a, and the values of $|AUX_1|$ and $|AUX_{-1}|$ will be increased. If the ratio of zeros and ones is still 1:1, the situation shown in Fig. 9b is satisfied, and $|AUX_{1/3}|$ and $|AUX_{-1/3}|$ will be increased.

The detailed workflow diagram of the threshold adaptive algorithm is shown in Fig. 10. In the adaptive module, the auxiliary reference voltage of the auxiliary sampler is first determined to obtain the corresponding decoded data. The decoded data are gray mapped to a certain number of logical zeros and logical ones. When the ratio of 0 to 1 meets 1:1, the determination of the average value of adjacent voltages will be performed; otherwise, the corresponding reference voltage will be adjusted according

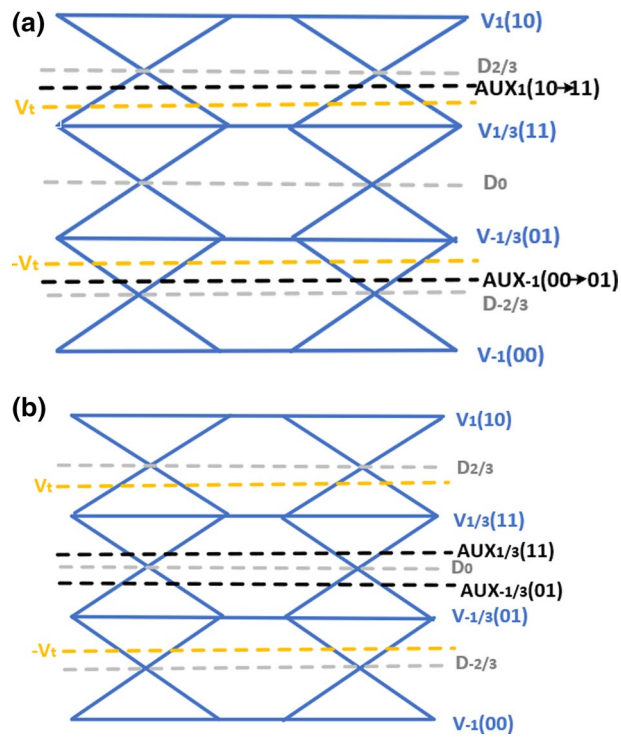

Fig. 9 ALP and AHN sampling results **a** large (red, green) and **b** small (yellow, black)

to the different percentages of 0 and 1. As can be seen from Fig. 10, the threshold adaptive scheme mainly uses Loop I and Loop II to adjust together to achieve the adaptive threshold, and only when the ratio of 0 and 1 in Loop I meets the condition, it will go to the next loop for adjustment. This loop nesting does increase the complexity of the algorithm to some extent, but with the joint adjustment of the two loops, it is able to maximize the adjustment of the offset thresholds, thus ensuring the accuracy of the placement of the bottom and top eye thresholds. Ideally, the auxiliary sampler adjacent level average lies exactly at the data threshold voltage $D_{2/3}$, satisfying $V_t = D_{2/3}$ and $-V_t = D_{-2/3}$.

3.2 Tap adaptation

The coefficients of the equalizer depend on the channel, and adaptive algorithms are often used to determine appropriate tap coefficients, while real-time adaptation of the equalizer coefficients can further improve robustness to channel variations. In this paper, the sign-sign least mean squares (SS-LMS) algorithm is used to adjust the tap coefficients, and the detailed tap adaptive flowchart is shown in Fig. 11. Here, *Da* is the voltage value sampled by the three data samplers (DH, DZ and DL) and *Em* is the error between the auxiliary reference voltage and the data reference voltage.

The tap adaptive algorithm is described as follows. As shown in Fig. 12, let $L_H(t)$, $L_Z(t)$ and $L_L(t)$ be the inputs of the DFE on the three paths after the output of the forward filter [20, 21]. The subscripts H, Z and L denote the paths of the sampler DH, DZ and DL, respectively. $D_H(t)$, $D_Z(t)$, $D_L(t)$ and $d_H(t)$, $d_Z(t)$, $d_L(t)$ are the DFE equalization

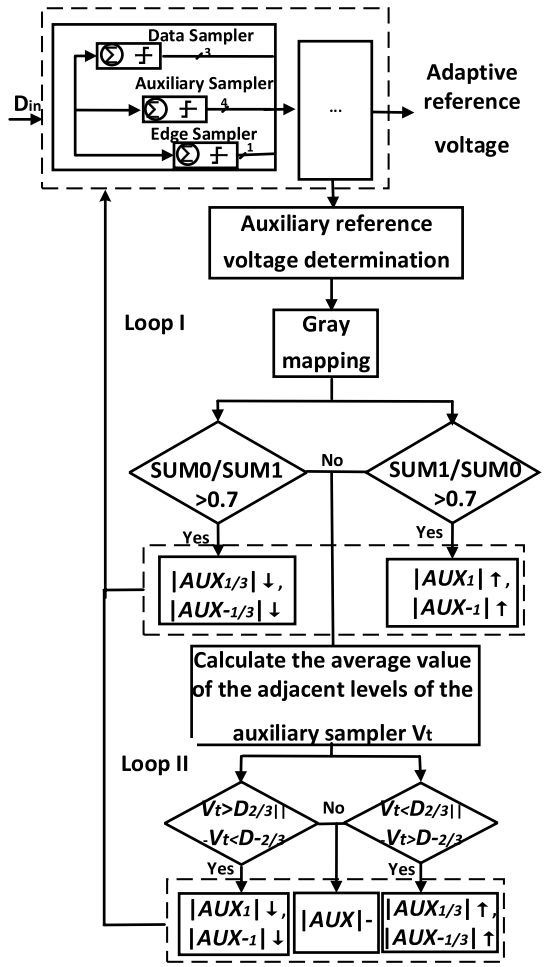

Fig. 10 Threshold adaptive flow chart

and feedback signals on the three paths, respectively. Let $d_{PAM4}(n)$ be the corresponding PAM4 signal after decoding. It follows that the input signal of this PAM4 DFE is

$$X(t) = L_H(t) + L_Z(t) + L_L(t) \tag{1}$$

The feedback signal of the DFE can be expressed as

$$F(t) = d_H(t) + d_Z(t) + d_L(t) \tag{2}$$

The DFE equalization signal can be expressed in terms of

$$\begin{aligned} Z(t) &= D_H(t) + D_Z(t) + D_L(t) = X(t) - F(t) \\ &= L_H(t) - d_H(t) + L_Z(t) - d_Z(t) + L_L(t) - d_L(t) \end{aligned} \tag{3}$$

Let h_i and f_i be the forward and feedback filter coefficients of the DFE, respectively. The input signal $X(t)$ is weighted and superimposed by the forward filter to obtain $Y(t, l)$:

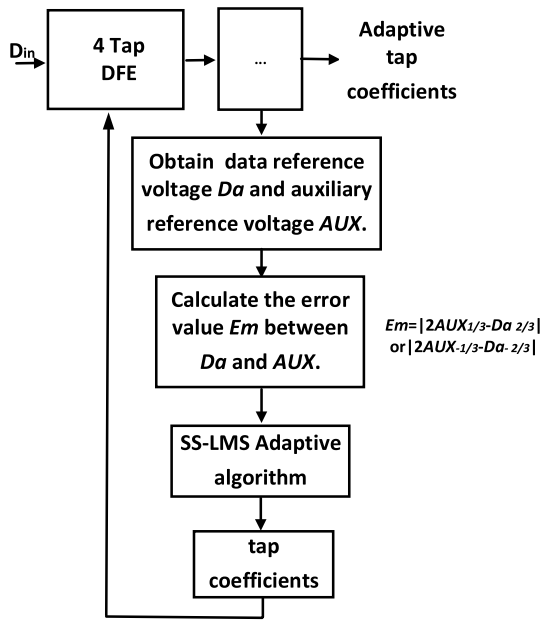

Fig. 11 Tap adaptive flowchart.

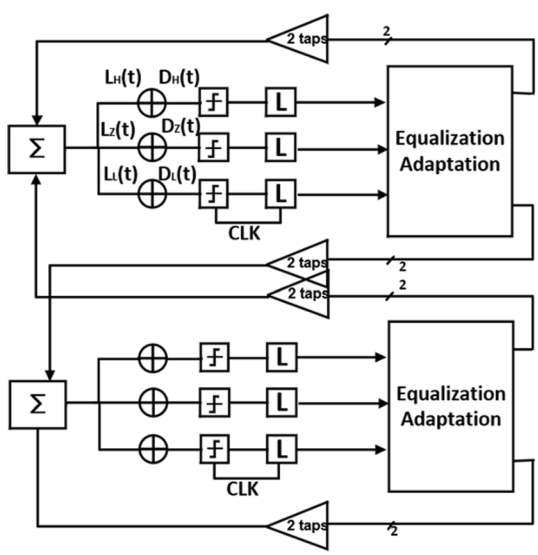

Fig. 12 Tap adaptation to each data path name

$$Y(t,l) = \sum_{i=1}^{N} h_i X(t-i,l) \tag{4}$$

where N is forward filter length and $X(t-i,l)$ is the DFE equalization information at the instant corresponding to the lth symbol period.

The error signal $e(t,l)$ can be expressed as follows

$$e(t,l) = D(t,l) - Y(t,l) \tag{5}$$

where $D(t,l)$ denotes the value of the signal expected to be received.

The received signal value $D(t,l)$ needs to be determined on the basis of the final decoding result $d_{PAM4}(n)$, since each symbol in PAM4 corresponds to a different value. Specifically, if $d_{PAM4}(n) = 1$, then $D(t,l) = 1$; if $d_{PAM4}(n) = 1/3$, then $D(t,l) = 1/3$; if $d_{PAM4}(n) = -1/3$, then $D(t,l) = -1/3$; and if $d_{PAM4}(n) = -1$, $D(t,l) = -1$.

Let the feedback signal obtained after the feedback filter be $F(t,l)$, then

$$F(t,l) = \sum_{i=1}^{L} f_i e(t-i,l) \tag{6}$$

where L is the length of the feedback filter.

The generated error signal and feedback signal are input to the DFE, and the equalization signal $Z(t,l+1)$ can be obtained, which is sampled by the sampling circuit to obtain the demodulated data symbol value of the PAM4.

The final weight coefficients h_i and f_i obtained by the SS-LMS algorithm are

$$\hat{h}_i(t,l+1) = h_i(t,l) + \mu e(t,l) Z(t-i,l) \tag{7}$$

$$\hat{f}_i(t,l+1) = f_i(t,l) + \mu e(t,l) F(t-i,l) \tag{8}$$

where μ is the step parameter.

4 System simulation and performance analysis

In this section, experimental simulation model of the proposed 112 Gb/s PAM4 transceiver architecture is built by MATLAB SIMULINK, and the experimental results are analyzed and compared with previous researches. At the transmitting end, the PRBS13 signal generated by the PAM4 code generator enters a channel with a loss of 25 dB after passing through a 3-tap FFE and a VGA. Then, at the receiving end, the signal after going through the lossy channel is equalized at the middle frequency, high frequency and low frequency by the three-stage CTLE, respectively. Figure 13a, b, c shows the corresponding CTLE transfer function curve. The 4-tap DFE will perform further operations on the amplified and partially equalized signal. Figure 14 shows the adaptive convergence process of the auxiliary sampler and the data sampler, where $Data_{2/3}$, $Data_0$ and $Data_{-2/3}$ represent the sampling voltages of the data sampler during the adaptive process, respectively. From Fig. 14, it can be seen that the four threshold voltages when the auxiliary sampler maintains dynamic balance are 170mv, 60mv, − 60mv and − 170mv, and the three threshold voltages when the data sampler reaches dynamic balance are 110mv, 0mv and − 110mv, respectively. This shows that the sampler threshold not only has a short convergence time during the adaptive process, but also has the same interval between the threshold voltages of each sampler when it reaches a steady state, which ensures that the output eye diagram has a good linearity.

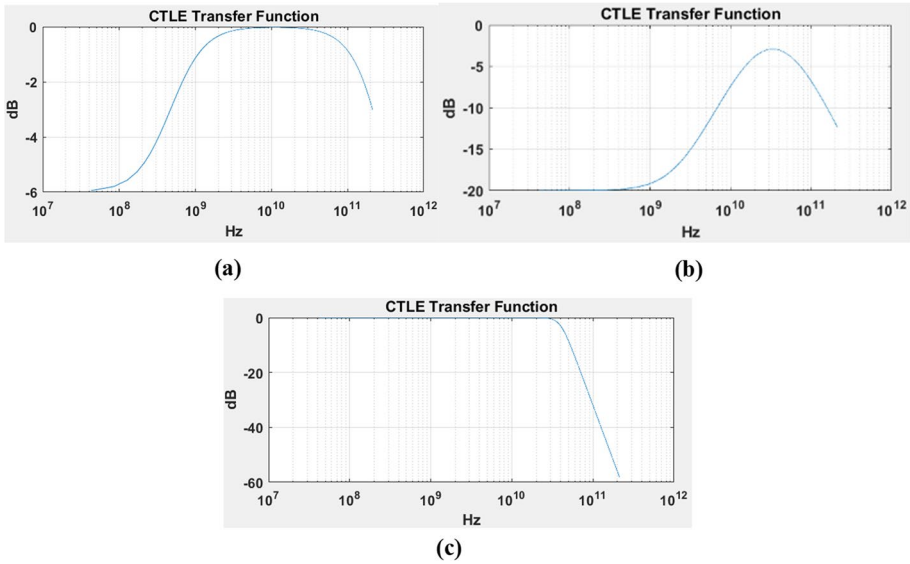

Fig. 13 Three-stage CTLE transfer function curve **a** mid-frequency, **b** high frequency, **c** low frequency

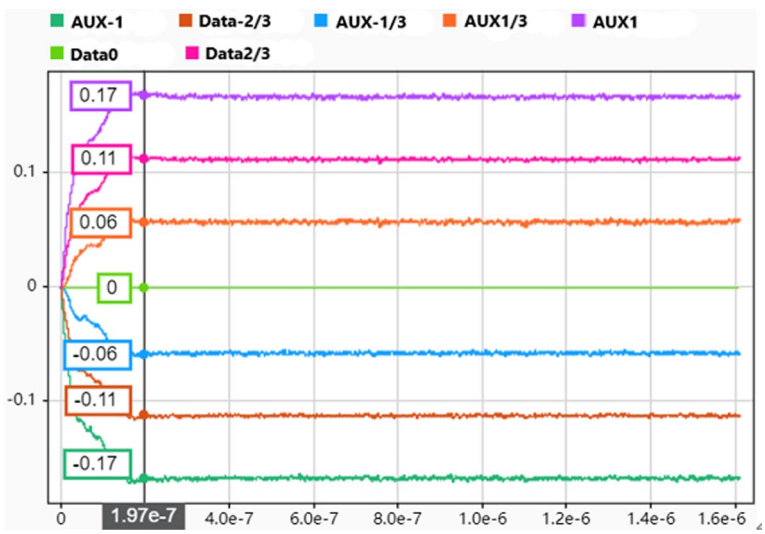

Fig. 14 Auxiliary and data sampler threshold adaptive convergence curve

Figure 15 shows the convergence view of the four taps of the DFE during the adaptation process. As can be seen from Fig. 15, all DFE taps are stable within 0.6us, with larger tap values for tap 1 and tap 2, and smaller tap values for tap 3 and tap 4. This shows that taps 1 and 2 have a greater impact on the ISI postscript. The unit impulse response before and after the transceiver equalization and the eye diagram at the receiver are shown in Fig. 16a, b. It can be clearly seen that the ISI leading and trailing of the equalized signal in Fig. 16a are significantly improved.

The proposed PAM4 transceiver design scheme has strong robustness, and its adaptive adjustment also allows the system to adapt well to different channel conditions. Figure 17a shows the variation of the average eye height of the eye diagram at

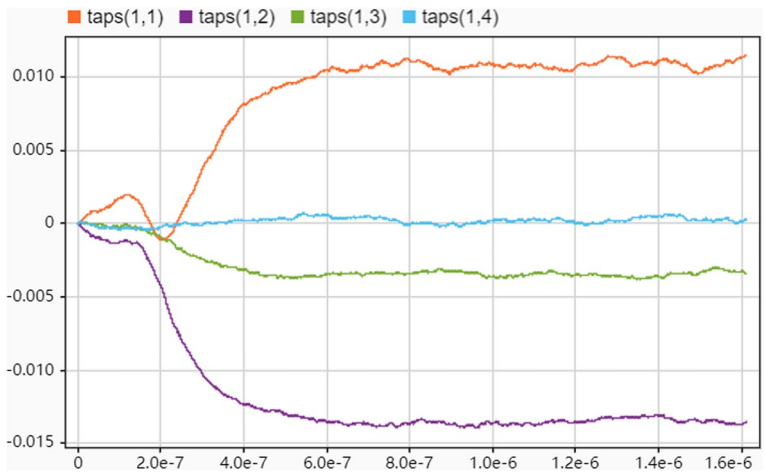

Fig. 15 Convergence view of the four taps of the DFE during the adaptation process

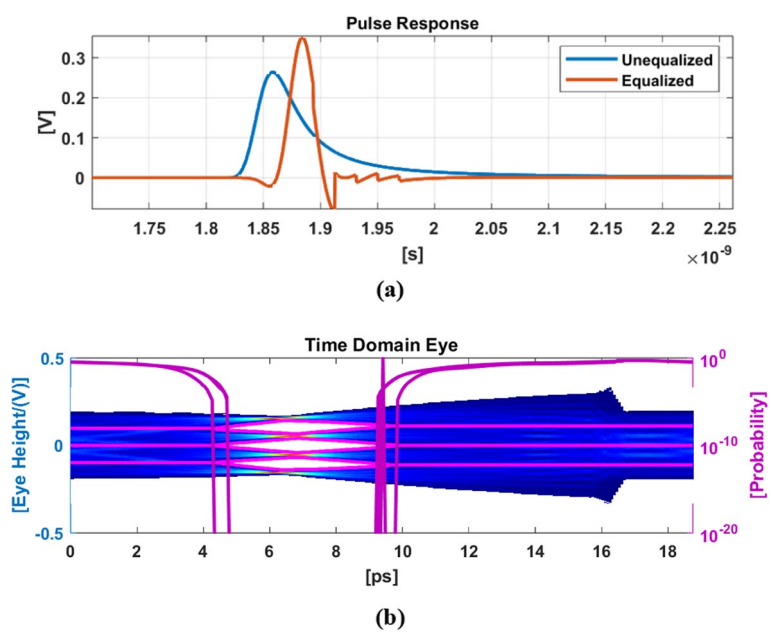

Fig. 16 **a** Unit impulse response and **b** eye diagram

the receiver with and without threshold adaption for different channel losses. From Fig. 17a, it can be concluded that the proposed scheme has good equalization capability in the range of channel loss of 10–25 dB, and the average eye height at the receiver end is above 59mv, while the performance of the eye diagram is greatly reduced without adaptive equalization. Figure 17b shows the variation of the average eye height at different channel losses when adding Gaussian noise with a noise power spectral density of 1×10^{-6} (V^2/GHz) to the input waveform. It is confident to conclude that this scheme has a significant performance improvement over the no-threshold adaptive scheme.

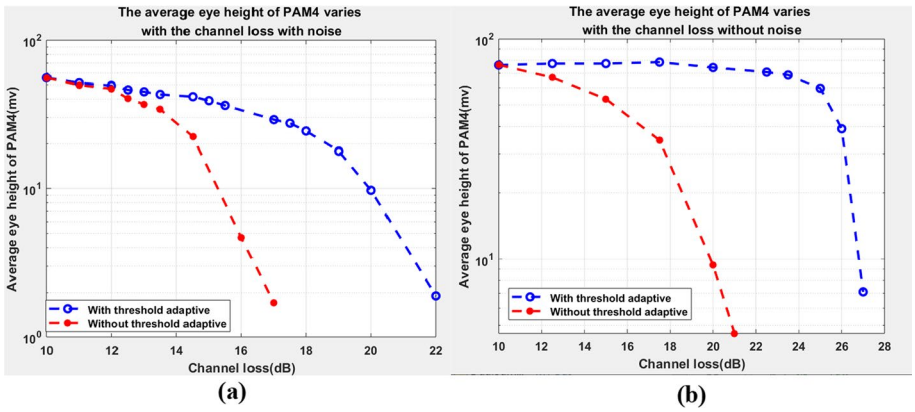

Fig. 17 Variation of average eye height with channel loss: **a** no noise added; **b** noise added

Table 1 PAM4 transceiver performance comparison

References	This Work	[13]	[1]	[12]	[22]
Data-Rate	112 Gb/s	56 Gb/s	40–56 Gb/s	112 Gb/s	112 Gb/s
Modulation	PAM4	PAM4	PAM4	PAM4	PAM4
TX Equalization	3-tap FFE	2-tap FFE	2-tap FFE	4-tap FFE	4-tap FFE
RX Equalization	3-stage CTLE and 4-tap DFE	1-stage CTLE and 1-tap FIR and 1-tap IIR DFE	2-stage CTLE and 10-tap DFE	2-stage CTLE and ADC-based 31-tap FFE and 1-tap DFE	3-stage CTLE and ADC-based 31-tap FFE and 1-tap DFE
Eye Height	59.6mv	14 mV	~20 mV	NA	NA
Eye width	0.27UI	0.19UI	~0.05UI	NA	NA
Channel Loss	25 dB	20.8 dB	10 dB	37.5 dB	20 dB
BER	10^{-12}	10^{-12}	10^{-12}	10^{-8}	2×10^{-5}
Supply	1 V	1.2 V	0.9 V/1.2 V/1.8 V	0.88 V/1.2 V/1.5 V	0.9 V/1.2 V/1.8 V

Table 1 compares the proposed scheme in this paper with some published research results. As can be seen from the table, at the same data rate, although the literature [12] can compensate for the higher channel loss, the design complexity and power consumption are larger due to the ADC architecture. In other schemes below 112 Gb/s, although the number of taps of the transmitting end FFE and the receiving end DFE in [13] is less than the proposed one, the eye diagram quality obtained by this proposed scheme is better than [13] and [1].

5 Conclusion

In this paper, a reliable 112 Gb/s PAM4 transceiver design scheme is proposed. Adaptation of sampler thresholds and DFE taps is introduced in the receiver to effectively compensate for channel loss in a more robust manner. In addition to this, low architecture complexity is achieved by improving the DFE structure on the receive side, and using only 3-tap FFE on the transmit side. The simulation results show that the proposed 112 Gb/s PAM4 transceiver transmits well on a channel with a loss of 25 dB and has better eye-diagram performance than previous researches with the same bit

error rate (10^{-12}), and the average vertical eye height and horizontal eye width are 59.6mv and 0.27UI, respectively. The design has significant reference value and strong application value.

Abbreviations

BER	Bit error rate
PAM4	Four-level pulse amplitude modulation
DFE	Decision feedback equalizer
CTLE	Continuous time linear equalizer
VGA	Variable gain amplifier
SatAmp	Saturation amplifier
SNR:	Signal–noise ratio
FFE	Feedforward equalizer
OIF	Optical Internetworking Forum
NRZ	Not-return-to-zero
DC	Direct current
ISI	Inter-symbol interference
ADC	Analog-to-digital converter
CDR:	Clock and data recovery
UI	Unit interval
AFE	Analog front end
SS-LMS	Sign-sign least mean squares

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Author contributions
XL is the first author. She developed and wrote the method presented in this paper. ZL participated in writing, reviewing and editing as a corresponding author. HW and MM participated in and guided the experimental process. Both YW and ZW were involved in the derivation of the equations in the revised manuscript. All authors read and approved the final manuscript.

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Declarations

Ethics approval and consent to participate
Not applicable.

Consent for publication
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Competing interests
The authors declare that they have no competing interests.

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