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Research Article

Adaptive Delta-Sigma Modulation for Enhanced Input Dynamic Range

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An adaptive delta-sigma modulator of 1st order with one-bit quantization is presented. Adaptation is instantaneous and based on an exponential law. The feedback signal is a multibit discrete-level signal generated by a digital-to-analog converter (DAC). Compared to a nonadaptive delta-sigma modulator of 1st order, the input dynamic range is significantly enhanced. The gain in dynamic range is 6 dB per bit defining the feedback amplitude. The influence of nonideal DAC performance is discussed. It is demonstrated that an implementation of the system is realistic with standard CMOS technology. To relax the requirements to the one-bit quantizer, the quantizer input signal is amplified adaptively (Q-Switching).

1. INTRODUCTION

Delta-sigma modulators (ΔΣMs) in general are used to convert analog waveforms to high-frequency, but low-resolution data sequences (sometimes designated "ΔΣ-sequences") [1, 2]. ΔΣMs inherently perform so-called noise shaping, whereby most of the quantization noise is shifted out of the base band toward higher frequencies, and thus the base band of the ΔΣ-spectrum contains the spectrum of the input signal plus some residual quantization noise. The quality of signal representation is characterized by the signal-to-noise ratio (SNR), which is the ratio of the signal power to the power of the residual base band noise. Assuming that the power of the residual noise in the base band is approximately constant and independent of the input amplitude, the SNR is directly proportional to the power of the input signal itself. Thus the SNR is decreasing for decreasing input amplitudes. The basic idea of adaptive ΔΣMs is to adapt the amplitude of the ΔΣ-sequence to the amplitude of the input signal such that the SNR roughly remains constant—at least within a specified range of input amplitudes. Various different types of adaptive ΔΣMs can be found in literature, for example, [3–9]. Adaptation algorithms based on "syllabic adaptation" [3, 4, 6, 7] are controlled by short time properties, for example, by the peak amplitude, within so-called "stationary periods" (typically between 10–30 milliseconds for speech, and about 5 milliseconds for music [4]) of the input. Adaptation algorithms based on the instantaneous signal amplitude ("instantaneous adaptation" [5]) have the advantages that they do not require a priori assumptions on the stochastic properties of the input, and that there is no delay in the adaptation response. Besides, less circuitry is necessary for implementation.

The input power in adaptive ΔΣM can be estimated directly from the input signal itself ("forward estimation" [6]), or from the modulator output ("backward estimation" [3–5, 7]).

The adaptive ΔΣM presented here is a single-bit system and uses *instantaneous adaptation* and *backward estimation*. The adaptation algorithm is based on an exponential law which ensures that the adaptation properties are independent of the average input power level over a particular input amplitude range. The feedback signal is generated by a digital-to-analog converter (DAC). Possible levels of the feedback signal are chosen from a finite set, which ensures a reproducible reconstruction of the input signal from the binary data sequence. The proposed adaptive modulator shows an improved peak SNR as compared to

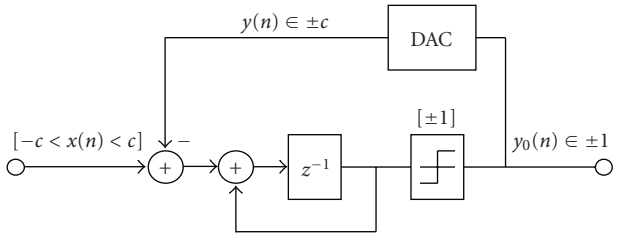

Figure 1: First order ΔΣM.

the nonadaptive version of the system. This is due to the instantaneous adaptation algorithm as presented here. In systems with syllabic adaptation, this effect does not occur, that is, the same peak SNRs are obtained for adaptive and nonadaptive versions [6, 7].

The system in [5] also describes an instantaneous adaptation algorithm and a DAC for feedback generation. However, this algorithm is based on a linear, instead of an exponential law, which limits the maximum adaptation speed. As compared to the proposed system, a clearly inferior performance is obtained in cases of "adaptation overload," that is, when the slope of the input signal is steeper than the maximum adaptation speed. Adaptation overload occurs, for example, when the input signal shows a sudden increase of signal power.

The adaptive ΔΣM [8] describes a step size adaptation algorithm which uses both sign and magnitude of the signal at the quantizer input. The current step size is increased, if the magnitude of the current quantizer input signal is larger than the previous step size, and decreased otherwise. While this algorithm yields a slightly improved peak SNR as compared to the system presented here (typically, between 3-4 dB), two bits are necessary for digital signal representation instead of only one bit for the system as presented.

Another adaptive ΔΣM is presented in [9]. However, the adaptation algorithm described here is primarily used to suppress tones close to half the sampling frequency, and not to enhance the input dynamic range. The SNR curve increases with increasing input amplitude level. As compared to the nonadaptive version of the ΔΣM, the dynamic range is extended by 2 dB toward higher input levels, and the peak SNR is improved by 5 dB.

2. ADAPTIVE ΔΣ MODULATION—ANALYSIS

2.1. Basic concept

The simplest ΔΣM, a nonadaptive modulator of 1st order, is depicted in Figure 1. An input signal $x(n)$ within the range of $[-c, +c]$ is converted to the binary output sequence $y_0(n) \in \pm 1$. Sequence $y_0(n)$ is converted to the "physical" feedback signal $y(n) \in \pm c$ by means of a 1-bit digital-to-analog converter (DAC). Here and in the following, physical and numeric representations of signals are distinguished by labeling numeric one or multibit signals with the subscript "0."

A ΔΣM of 1st order can generally be regarded as a linear (nonadaptive) delta-modulator, whose input is $\sum_n x(n)$, that is, the accumulated input $x(n)$. If the input is within the range of $[-c < x(n) < +c]$, the magnitude of the maximum slope of the accumulated sequence $x(n)$ is smaller than c/T (with T as sampling period). Thus, the delta modulator can theoretically always track its input, and the so-called "slope-overload conditions" cannot occur. In this model, parameter "c" represents the step size of the prediction signal $\sum_n y(n) = c\sum_n y_0(n)$, which tracks the accumulated input $\sum_n x(n)$. Condition $|x(n)| < c$ is necessary and sufficient for the elimination of slope-overload situations.

In an adaptive ΔΣM with instantaneous adaptation, step size c is not fixed, but adapted to the local *magnitude* of the input, $c \rightarrow c(n)$. To avoid slope-overload, condition

$$|x(n)| < c(n) \tag{1}$$

has to be fulfilled at any time.

A block diagram of the adaptive ΔΣM as proposed here is shown in Figure 2. It contains the subtract-and-accumulate stage typical for 1st order ΔΣ modulation, and a 1-bit quantizer. In the adaptation stage, the quantizer output $y_0(n)$ is used to generate a multibit step size amplitude $c_0(n)$. The numeric output of the system is the signal $z_0(n) = y_0(n)c_0(n)$. The physical signal $z(n) = \pm c(n)$, which is used as feedback signal, is generated by a DAC. If $c_{\max}$ is the maximum (physical) step size, the range of the input signal is given by $[-c_{\max} < x(n) < c_{\max}]$.

The output $v(n)$ of the accumulator is multiplied by a factor $d(n)$, which is derived from $c_0(n)$ in a stage "Q-Switching." However, since the quantizer detects only the sign of $v(n)$, this multiplication plays a role only if the practical implementation of the system is regarded (cf. section "*Q-Switching*").

Step size $c_0(n)$ at a particular time instant is controlled by a set of code words $[y_0(n), y_0(n-1), y_0(n-2), \ldots]$, which are the instantaneous and a particular number of previous code words. The way the adaptation stage works is intuitively clear. Amplitude $c(n)$ needs to be increased, if the set $[y_0(n), y_0(n-1), y_0(n-2), \ldots]$ is composed of equal code words. In this case, $|x(n)|$ tends to exceed $c(n)$, which would violate condition (1). On the other hand, $c(n)$ should be decreased, if the set $[y_0(n), y_0(n-1), y_0(n-2), \ldots]$ shows an alternating pattern of code words.

The step size adaptation algorithm presented here is based on an exponential law. If the input signal shows an abrupt transition from high to low amplitudes, then step size sequence $c_0(n)$ is decaying roughly exponentially, where neighboring step sizes differ by about a factor $\alpha < 1$, that is,

$$c(n) \approx \alpha c(n-1). \tag{2}$$

The decay is not perfectly exponential, since step sizes $c(n)$ are generated by a DAC, and thus $c(n)$ is subjected to a rounding procedure. To determine the size of α it is assumed that the step size decay is approximating the impulse response of a low-pass filter of 1st order, where the cutoff frequency is equal to the base band limit W. A short calculation shows that α can be expressed as a function of the

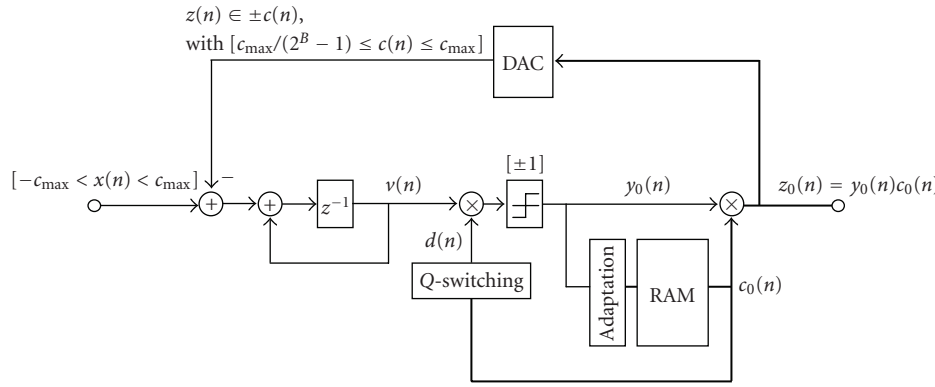

Figure 2: Adaptive ΔΣM of first order.

oversampling ratio OSR $= 1/(2WT)$ (with ΔΣ clock period T)

$$\alpha = \exp\left(-\frac{\pi}{\mathrm{OSR}}\right). \tag{3}$$

The step sizes are generated by a DAC comprising B magnitude bits and one sign bit, and thus the numeric step sizes $c_0(k)$ have to be represented by a finite set of integer numbers within the range $[2^B - 1 \ge c_0(k) \ge 1]$. Assuming index k within the range $[0 \le k \le k_{\max}]$, step sizes $c_0(k)$ are obtained by rounding the continuous-valued numbers of function $(2^B - 1)\alpha^k$ to the next integers, that is,

$$c_0(k) = \mathrm{round}((2^B - 1)\alpha^k). \tag{4}$$

The maximum step size at $k = 0$ is $c_0(0) = 2^B - 1$. Since the minimum step size is 1, sequence $c_0(k)$ is truncated at index $k_{\max}$. The condition for truncation is

$$(2^B - 1)\alpha^{k_{\max}} > \frac{1}{2}, \tag{5}$$

resulting in

$$k_{\max} = \mathrm{floor}\left(-\frac{\ln(2(2^B - 1))}{\ln(\alpha)}\right). \tag{6}$$

Indices $k > k_{\max}$ would yield step sizes equal to zero, which does not make sense in the present application. The set of step sizes $c_0(k)$ comprises an overall number of $k_{\max} + 1$ numbers which approximate an exponentially decaying function if k is increased from $k = 0$ to $k = k_{\max}$. In the present system, all step sizes are stored in a look-up-table RAM at addresses from $k = 0$ to $k = k_{\max}$. In a running modulator, changing of step sizes is achieved by simply shifting the instantaneous RAM-address to higher addresses for step size decrease, and to lower addresses for step size increase.

An example of an adaptation algorithm has been determined empirically for best SNR performance, assuming a 9-bit DAC ($B = 8$) and an oversampling ratio of OSR $= 50$. The numeric signals $z_0(n)$ and $c_0(n)$ are composed of 9 bits and 8 bits, respectively. With (3), the exponential base is $\alpha = 0.9391$, and with (6), $k_{\max} = 99$, that is, 100 step sizes are stored in the RAM. The exact integer values of $c_0(n)$ are defined by (4). As shown in Table 1, the step size is decreased by about a factor α^1 (i.e., RAM address increased by 1 position) if four consecutive code words have alternating signs, and increased by approximately a factor α^{-3} (i.e., RAM address decreased by 3 positions) if five consecutive code words are equal. The increase of $c(n)$ occurs considerably faster than the decrease, since violation of condition (1) has to be avoided by all means. Empirically, a factor α^{-3} has proven to be sufficient.

Sample waveforms for an adaptive ΔΣM implementing the adaptation algorithm described in Table 1 are shown in Figures 3 and 4. The first trace in Figure 3 depicts an example of an input signal $x(n)$. The second trace shows the full wave rectified version $|x(n)|$ together with the magnitude $c(n) = |z(n)|$ of the DAC-output signal. The third trace illustrates the full DAC-output signal $z(n)$. In Figure 4, signal $x(n)$ is attenuated by 40 dB as compared to Figure 3. As expected, the quantization of signals $c(n)$ and $z(n)$ appears more pronounced. The examples in Figures 3 and 4 demonstrate that the step size adaptation algorithm works instantaneously, that is, the feedback amplitude $c(n)$ tracks the individual maxima and minima of $|x(n)|$.

Figure 5 depicts the SNRs of various types of analog-to-digital converters as a function of the input signal power. The input $x(n)$ within the range of $[-1, +1]$ is a periodic, zero-mean noise sequence composed of $N = 4000$ samples. Within a bandwidth $W = 10$ kHz, amplitudes and phases of the spectral lines are randomized. Different signal power levels are obtained by scaling this signal. The input power is referred to the power level of a dc-signal with amplitude +1. The sampling rate for all simulations is $1/T = 1$ MHz (OSR $= 50$), and the SNRs are computed within base band W.

Curve (1) depicts the SNR of an ideal adaptive ΔΣM, where the adaptation algorithm of Table 1 and a 9-bit DAC ($B = 8$ magnitude bits, one sign bit) are used ($c_{\max} = 1$). The SNR is about 50 dB and remains quite constant between the maximum input power down to about −50 dB. For lower input power levels, the SNR decreases. Curve (2) shows the SNR of an ideal nonadaptive ΔΣM of 1st order with

Table 1: Adaptation algorithm.

Code	Step size multiplier ($\alpha < 1$) $[0 \le k(n) \le k_{\max}]$
$y_0(n) = y_0(n-1) = y_0(n-2) = y_0(n-3) = y_0(n-4)$	$c_0(n) = \text{round}((2^B - 1)\alpha^{k(n-1)-3})$
$y_0(n) = -y_0(n-1) = y_0(n-2) = -y_0(n-3)$	$c_0(n) = \text{round}((2^B - 1)\alpha^{k(n-1)+1})$
Other combinations	$c_0(n) = c_0(n-1) = \text{round}((2^B - 1)\alpha^{k(n-1)})$

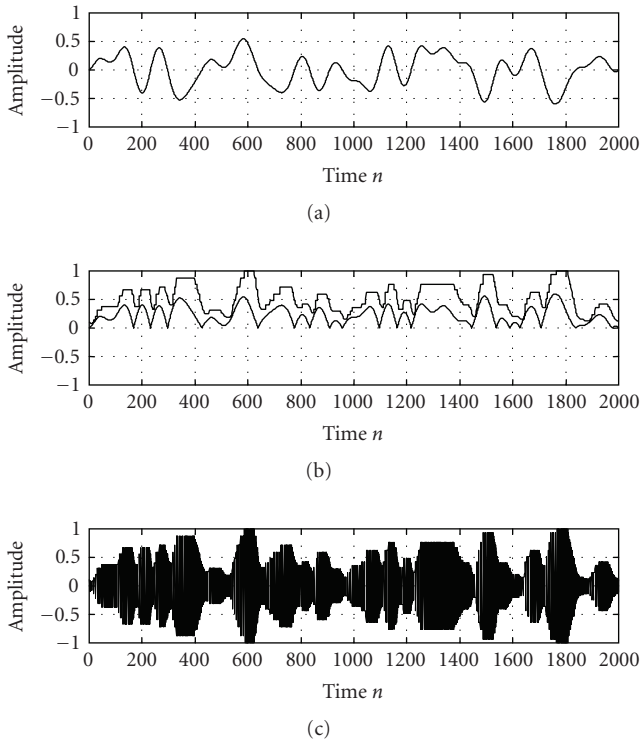

Figure 3: Example waveforms derived from an adaptive ΔΣM modulator of first order. First trace: input signal $x(n)$. Second trace: rectified input signal $|x(n)|$ and feedback amplitude $c(n)$ (note: $c(n) > |x(n)|$). Third trace: output signal $z(n)$.

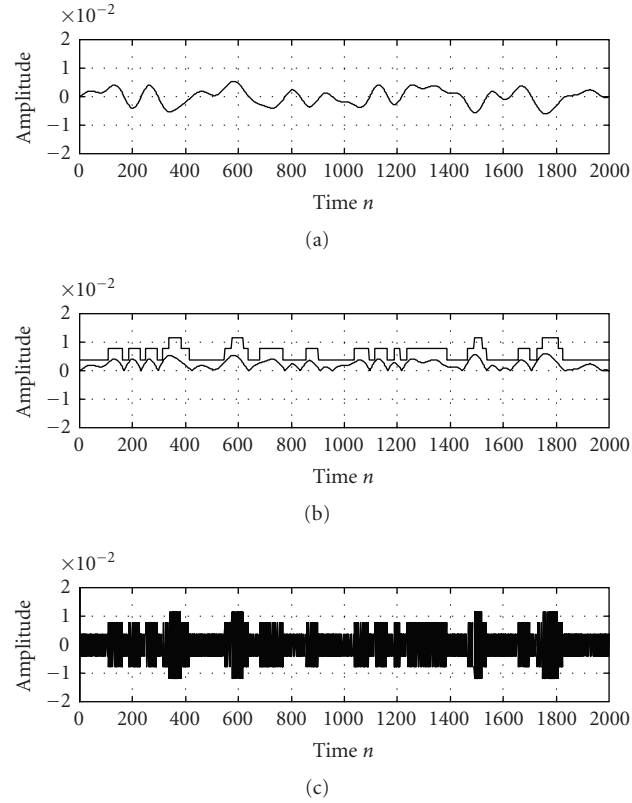

Figure 4: Waveforms as shown in Figure 3, but input signal $x(n)$ attenuated by 40 dB.

$c(n) = c_{\max} = 1$. Obviously, the segment of curve (2) at low input levels is very similar to curve (1), shifted to the left by 48 dB. In this region, the adaptive ΔΣM operates equal to a nonadaptive ΔΣM with the minimum step size $c(n) = c_{\min} = 1/255$. Note that compared to the nonadaptive ΔΣM, the input dynamic range of the adaptive ΔΣM is expanded by approximately 48 dB, corresponding to 6 dB per magnitude bit in the feedback DAC signal. In addition, the peak SNR is improved by about 6 dB. This improvement of peak SNR is due to the instantaneous adaptation algorithm, where the amount of quantization noise introduced into the system is adaptively controlled by the local magnitude of $|x(n)|$. Hence, less noise power is introduced as compared to the cases with constant (i.e., no adaptation) or very slowly varying (i.e., syllabic adaptation) feedback amplitude. Curve (3) depicts the SNR of a 2nd order ΔΣM. While the SNR peak of curve (3) is better than the one of curve (1), for input levels below about −30 dB, the adaptive ΔΣM clearly outperforms the 2nd order system. Curves (4) and (5) depict the SNRs of pulse code modulation (PCM) systems with 13- and 14-bit resolution. Whereas the 14-bit PCM system is superior to the adaptive ΔΣM for all input levels, the 13-bit PCM system is inferior at least at low-level input signals.

Simulations have also been carried out with pure sinusoidal input signals, and different frequencies have been examined. However, the results are not depicted, since they are qualitatively very similar to the results shown in Figure 5.

2.2. Influence of DAC imperfections

A nonideal DAC can be regarded as an ideal DAC plus a noise source. Unfortunately, the noise contributes directly to the noise energy in the base band of the ΔΣM output, because no noise shaping effects take place. Thus, the properties of the DAC have critical influence on the performance of the adaptive ΔΣM.

In Switched-Capacitor (SC) technology, DAC accuracy depends primarily on capacitor matching. In state-of-the-art

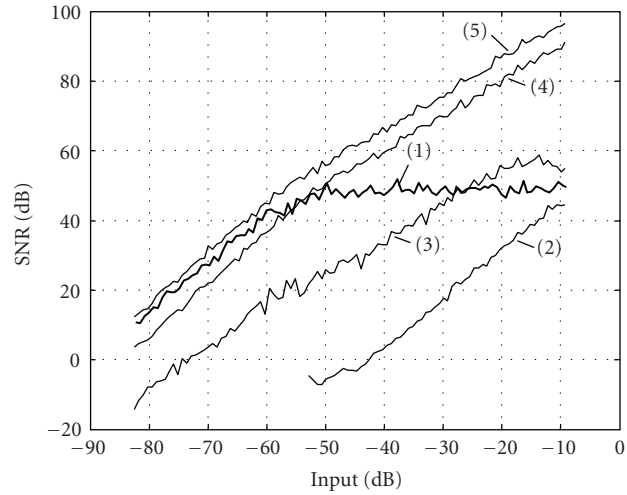

Figure 5: SNR for different ideal analog-to-digital converters. Input signals are band limited zero-mean noise signals with $B = 10\,\text{kHz}$ ($N = 4000$). Curve (1): adaptive ΔΣM (9-bit DAC). Curve (2): nonadaptive ΔΣM of first order. Curve (3): nonadaptive ΔΣM of second order. Curve (4): 13-bit PCM. Curve (5): 14-bit PCM.

CMOS processes, capacitor matching is dominated by oxide variations resulting in

$$\sigma\left(\frac{\Delta C}{C}\right) = \frac{A_C}{\sqrt{\text{area}}}, \tag{7}$$

where σ is the standard deviation of the relative error $\Delta C/C$, and A_C is a process-dependent constant [10]. Simulations have been carried out to estimate the influence of capacitor mismatch, taking the technology parameters of a typical $0.35\,\mu$m CMOS process. A 9-bit DAC with 1 sign bit $y_0(n)$ and 8 magnitude bits $c_0(n)$ is assumed, where the magnitude bits are represented by 8 binary weighted capacitors. The LSB capacitor with 25 fF requires an area of $29\,\mu\text{m}^2$. Taking a typical value $A_C = 0.45\%\,\mu$m, (7) yields $\sigma_{\text{LSB}} = 0.08\%$. The MSB capacitor which is 128 times larger requires an area of $3712\,\mu\text{m}^2$ and yields a considerably smaller standard deviation $\sigma_{\text{MSB}} = 0.007\%$. Note that the *relative error* is decreased, although the *absolute error* is increased. The simulations show that for $\sigma_{\text{LSB}} < 0.3\%$ there is only negligible influence on the SNR performance as depicted in curve (1) in Figure 5. The performance starts to decrease for $\sigma_{\text{LSB}} > 0.3\%$, and first signs of degradation appear in the region around the "SNR knee" for an input signal in the range of $[-60\,\text{dB}, -40\,\text{dB}]$.

2.3. *Q*-switching

The adaptive ΔΣM concept described herein imposes additional requirements on the specifications of the comparator, that is, the 1-bit quantizer. In practical implementations of comparators, the response time usually increases with decreasing input voltage difference. In ΔΣMs, too small comparator input differences might cause comparator failures resulting in bit errors in the data stream. If those failures appear sporadically (single bit errors), they cause only negligible SNR degradation, and the ΔΣ concept in general is known to be robust against such errors. However, the density of failures must not exceed a particular limit.

Table 2: Adaptation scheme for *Q*-switching.

Step size $c_0(n)$ in binary representation	Overall capacitance $C_{\text{ACC,TOT}}(n)/C_{\text{ACC}}$	Factor $d(n)$
[1 x x x x x x x]	128	1/128
[0 1 x x x x x x]	64	1/64
[0 0 1 x x x x x]	32	1/32
[0 0 0 1 x x x x]	16	1/16
[0 0 0 0 1 x x x]	8	1/8
[0 0 0 0 0 1 x x]	4	1/4
[0 0 0 0 0 0 1 x]	2	1/2
[0 0 0 0 0 0 0 1]	1	1

"x" denotes "don't care"

In an adaptive ΔΣM, the probability for comparator failures is dramatically increased for low power input signals. Here, the feedback amplitude $c(n)$ is small (cf. Figure 4), and thus the mean signal amplitude at the comparator input is also small. "*Q*-Switching" as described in the following is an approach to relax this problem.

The practical SC-realization of an adaptive ΔΣM as shown in Figure 2 usually involves a subtract-and-accumulate circuit consisting of an operational amplifier (opamp) with an integration capacitor, and capacitors for sampling the input signal (input capacitor) and the feedback signal (DAC-capacitors) (examples, e.g., in [1]). In the *Q*-Switching approach, the single integration capacitor is replaced by a variable capacitance. The basic idea is to adapt the integration capacitance to the instantaneous input signal power. For example, in Figure 6 an overall integration capacitance $C_{\text{ACC,TOT}}(n)$ can be configured by means of an array of capacitors $C_{00}, C_0, C_1, \ldots, C_6$. An example for an adaptation algorithm is summarized in Table 2. $C_{\text{ACC,TOT}}(n)$ is derived from the position of the first logical "1" in the bit pattern of feedback magnitude $c_0(n)$, while bits at less significant positions (labeled "*X*") are ignored. This method provides a rough estimate of the input signal amplitude and can easily be implemented. Capacitance $C_{\text{ACC,TOT}}(n)$ decreases with decreasing input signal amplitude. Factor $d(n)$ is proportional to the inverse of $C_{\text{ACC,TOT}}(n)$ (cf. Figure 2).

Each ΔΣ clock period consists of a "sampling section" and an "accumulation section." During the sampling section, the input capacitor and the DAC-capacitors are disconnected from the opamp and charged up by $Q_{\text{in}}(n)$ (proportional to the input signal $x(n)$) and $Q_{\text{DAC}}(n)$ (proportional to the (negative) feedback signal $-z(n)$). During the accumulation section, the sum of the charges is forced to flow into the integration capacitance, that is, its charge changes to $Q_{\text{in}}(n) + Q_{\text{DAC}}(n)$. The sign of the new potential at the output of the operational amplifier referred to a reference potential V_{ref} is detected by the comparator, and clocked into a flip-flop at the end of the accumulation section. Charge accumulation and

sign detection have to be finished within the accumulation section, and therefore the response time of the comparator has to be shorter than 50% of one ΔΣ clock period.

The integration capacitance is adapted during the sampling section of a ΔΣ clock period, that is, the preparation of charges $Q_{\text{in}}(n)$ in the input sampling capacitor, and $Q_{\text{DAC}}(n)$ in the DAC are not affected. Two cases have to be distinguished, (i) an uncharged capacitor is added to, and (ii) a capacitor removed from the instantaneous configuration. One port of each capacitor of the array is permanently connected to the inverting input of the amplifier.

(i) An uncharged capacitor can simply be added to the array $C_{\text{ACC,TOT}}$ by connecting its switched port to the amplifier output. This causes a redistribution of the charges and thus a change in the voltage U_{ACC}. For example, if capacitor $C_1 = 2C_{\text{ACC}}$ is added to the active array, voltage U_{ACC} changes from $Q_{\text{ACC}}/C_{\text{ACC,TOT}}$ to $Q_{\text{ACC}}/(C_{\text{ACC,TOT}} + 2C_{\text{ACC}})$, where Q_{ACC} is the charge in the active array in the sampling section. The magnitude of U_{ACC} is decreased in this case, since the overall capacitance has been increased at a constant charge.

(ii) Removing a capacitor from the active array is achieved by connecting its switched port to the reference voltage V_{ref}. Since this potential is equal to the virtual potential of the inverting input of the amplifier, the amplifier forces the output to change its potential. For example, if capacitor $C_2 = 4C_{\text{ACC}}$ is removed, voltage U_{ACC} changes from $Q_{\text{ACC}}/C_{\text{ACC,TOT}}$ to $Q_{\text{ACC}}/(C_{\text{ACC,TOT}} - 4C_{\text{ACC}})$. As above, Q_{ACC} is the charge in the active array in the sampling section. The magnitude of U_{ACC} is increased in this case, since the overall capacitance has been decreased at a constant charge.

Note that for system performance, the exact value of $C_{\text{ACC,TOT}}$ is not critically important. The two essential requirements for the adaptation algorithm are that first, on average, the magnitude of voltage U_{ACC} is maximized without exceeding specified limits, and second, switching between different configurations of $C_{\text{ACC,TOT}}$ has to be performed *without any loss of charge* (thus, the name *Q*-Switching). Any loss of charge in $C_{\text{ACC,TOT}}$ would result in accumulation errors and thus degrade system performance.

3. SUMMARY

The essential properties of the proposed adaptive single-bit ΔΣMs may be summarized as follows.

(1) The adaptation is "instantaneous" and controlled by a very small number of single bit code words (five for increase, and four for decrease of step sizes, cf. Table 1). There is no need for computing short time power estimates or envelopes of the input as typically required in "syllabic" adaptation algorithms.

(2) The adaptation scheme is based on an exponential law, and for implementation, a DAC comprising B magnitude bits and one sign bit is used. Compared to a nonadaptive ΔΣM of 1st order, the overall gain in input dynamic range is about 6B dB.

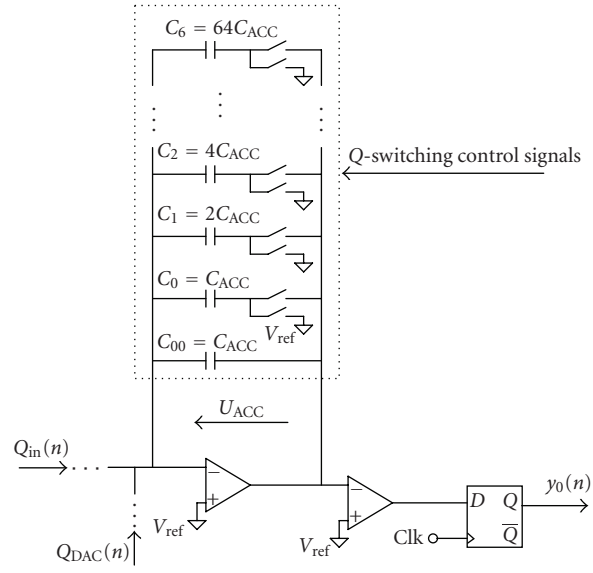

Figure 6: Charge accumulation with variable integration capacitance ("Q-Switching").

(3) In addition to the enhanced input dynamic range, an improvement of the peak SNR of about 6 dB is obtained. This improvement is due to the instantaneous adaptation. Since the feedback amplitude $c(n)$ tracks the individual maxima and minima of magnitude $|x(n)|$, on average less quantization noise is introduced as compared to systems based on syllabic adaptation.

(4) It is recognized that an increased input dynamic range imposes special requirements to the 1-bit quantizer. In SC-technology, *Q*-switching provides a means to relax this problem.

(5) The system can be implemented using standard SC-technology. Simulations show that state-of-the-art accuracy for the implementation of the DAC is sufficient to achieve the theoretically predicted SNR.

As a practical example, the proposed adaptive ΔΣM is successfully implemented in a cochlear implant system manufactured by Medical Electronics (MED-EL) in Innsbruck, Austria. A 9-bit modulator has been integrated in SC-technology for analog-to-digital conversion of the audio signal. The modulator is part of the so-called "speech processor," that is, the nonimplanted part of a cochlear implant system, which is used to operate the implanted stimulator [11]. The SNR curve (1) in Figure 5 perfectly meets the requirements in this medical application for hearing impaired subjects. The dynamic range of the audio signal is about 80 dB, and a peak SNR of about 50 dB within a frequency range of $W = 10$ kHz is sufficient for subsequent implementation of various stimulation strategies. At present,

about 7500 speech processors utilizing the proposed adaptive ΔΣM are in practical use.

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