

Editorial

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In the past years, digital signal processing (DSP) algorithms and architectures for baseband communication systems have fuelled the delivery of applications such as 3G mobile communications and wireless LAN to mass markets. This was made possible by a tremendous growth in the performance of computational devices such as digital signal processors and FPGAs, as well as an increase in sampling rates of conversion devices to potentially several 100 MHz. While the development of both computational devices and ADCs/DACs continues, thus permitting DSP to be applied at IF sampling rates and possibly beyond, the opportunities for further enhancing radio devices by DSP algorithms and architectures arise.

Against this background of development, an IEE/EURASIP conference on “DSP-Enabled Radio” was held at the Institute for System Level Integration (ISLI) in Livingston, Scotland, in September 2003. This very lively one-and-a-half-day event brought together 120 researchers from both industry and academia with a strong international participation. It was the spirit of this DSP-Enabled Radio conference and the contributions therein that brought to life the idea to this special issue. This issue contains both contributions from the event and responses to an open call for papers.

Naturally, the topic of signal processing for radio and communications admits a wide range of research. The papers of which this special issue comprises firstly address general design approaches, tools, and methods to develop DSP-based radio systems. A second group of papers reports on system implementations, which include devices running on both dedicated hardware and PCs, and application areas as diverse as multimedia and astronomy. A third group

discusses specific DSP algorithms which can be accommodated by communications systems based on digital processing platforms. A brief summary of the respective contributions is presented below.

GENERAL DESIGN APPROACHES AND TOOLS

The first five papers address design issues, approaches, and tools related to complex communications systems. P. Belanović et al. address the problem of the design gap, and argue for automatic approaches to virtual prototyping. The proposed scheme aims at a very short automated stage producing a virtual prototype, which outlines both the hardware and software of the final design. Subsequently, in the final stage of the design cycle, hardware and software implementation can be performed concurrently, leading to a considerably reduced overall design time. An example for a UMTS system is provided. K. van Berkel et al. present an embedded vector processor, which aims at integrating a large number of baseband DSP functions into a single architecture. The flexibility of this approach is demonstrated by a number of examples across various standards, including mobile and wireless, that may be operated on such a device. X. Revés et al. discuss the implementation of DSP radio functions on various platforms via a hardware-independent abstraction layer, which offers a common interface across the different systems. Built on this interface are three blocks which together can implement and execute radio functionality in real time. The paper by E. Senn et al. is concerned with estimating the power and energy consumption of a DSP algorithm given in C-code when executed on a variety of computational platforms. This modelling tool allows designers to consider the effect of processor

and algorithm choice on the overall power consumption at an early stage in system design. Based on the analysis of several central communications functions such as scrambling, puncturing, and interleaving, S. H. Jeong et al. propose the inclusion of a dedicated functional unit to execute bit manipulations into a digital signal processor. Results underline the benefit of this approach through the ability to considerably reduce the number of clock cycles compared to a standard digital signal processor if such a functional unit for bit manipulations is employed.

SYSTEMS AND HARDWARE

The next section of papers in this special issue report system implementations and specific hardware for reconfigurable radios. Of the first three radio implementations, the paper by R. Schiphorst et al. presents a software-defined radio system realised on a Pentium 4 processor platform equipped with additional ADC and DAC functionality. The approach is interesting, since the proposed solution leaves the standard route of dedicated processor platforms and moves to very commonly available general-purpose processors, on which both Bluetooth and a HiperLAN/2 specification are implemented and jointly operated. R. Mostafa et al. report on the architecture of their software-based MIMO prototype system, which implements space-time block coding and similar MIMO techniques. Their study is supported by channel and capacity measurements using their system. An astronomical application of a software-defined radio system is discussed in the paper by R. Weber et al. Motivated by the need for accurate power spectral density estimation in the astronomic radio spectrum corrupted by considerable levels of interference, they present the implementation of a powerful front-end platform and its application to resolve a specific astronomical radio source.

The latter two papers in this section address system components. With respect to baseband processing, I. Barbieri et al. discuss a system-on-chip of a multimedia application exemplarily comprising of a video and speech coder. The design focuses on the general design procedure of a hardware/software codesign and the reconfigurability of such a system. On the RF side of the radio front-end, S.-H. Oh et al. introduce an antenna design which can be electronically tuned towards various frequency bands. In their example, they demonstrate an antenna that can cover various GSM, DCS, and PCS bands with good narrowband characteristics by controlling the antenna parameters from the baseband digital signal processor.

ALGORITHMS FOR DSP-ENABLED RADIOS

The remaining papers in this special issue discuss advanced signal processing solutions, which are motivated by the availability of a software-based radio system. The first two papers in this section address blind synchronisation and equalisation in DSP-based transmission systems. M. Valkama et al.

consider the synchronisation, equalisation, and carrier offset compensation based on a blind source separation scheme applied to the inphase and quadrature components of the received signal, which is particularly aimed at direct conversion receivers. C. Tibenderana and S. Weiss address a Bluetooth receiver, which utilises the availability of a high-performance computing platform required for wireless LAN applications in order to obtain significant increases in quality when targeting Bluetooth. The performance benefit could translate into an increase in the distance over which Bluetooth can operate, or into an increase in throughput.

The last two papers utilise the availability of antenna arrays in the radio transceiver system. K. D. Le et al. investigate the relative impacts of fixed and adaptive processing using multiple receive antennas for a WLAN application using OFDM modulation. The evaluation relies on a new three-dimensional stochastic indoor propagation model. G. W. Rice et al. survey the estimation and performance of a 2D-RAKE receiver in a temporally and spatially dispersive fading channel. Both coherent and noncoherent solutions to parameter tracking are proposed, and their benefit from transmit diversity investigated.

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Michael W. Hoffman received the B.S. degree from Rice University, Houston, Texas, the M.S. degree from the University of Southern California, Los Angeles, and the Ph.D. degree from the University of Minnesota, all in electrical engineering. From 1985 to 1988, he was a signal processing system engineer in the Space Communications Division, TRW Inc. In 1993, he joined the University of Nebraska-Lincoln, where he currently serves as an Associate Professor. His research interests include data compression, joint source-channel coding, and sensor array processing.



Stephan Weiss received the Dipl.-Ing. degree from the University of Erlangen-Nürnberg, Erlangen, Germany, in 1995, and the Ph.D. degree from the University of Strathclyde, Glasgow, Scotland, in 1998, both in electronic and electrical engineering. In 1999, he joined the Communications Research Group within the School of Electronics and Computer Science at the University of Southampton, where he is a Senior Lecturer. Prior to this appointment he held a Visiting Lectureship at the University of Strathclyde. In 1996/1997, he was a Visiting Scholar at the University of Southern California. His research interests are mainly in adaptive and array signal processing, multirate systems, and signal expansions, with applications in communications, audio, and biomedical signal processing. For his work in biomedical signal processing, he was a corecipient of the 2001 Research Award of the German Society on Hearing Aids. He is a Member of the VDE and EURASIP, a Senior Member of the IEEE, and a Member of the IEE Signal Processing Professional Network Executive Team.

