EURASIP Journal on Applied Signal Processing 2002:9, 877–878

Editorial

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The telecommunications, wireless communications, multimedia, and consumer electronics industries are witnessing a rapid evolution toward integrating complete systems on a single chip. Single-chip systems will increasingly have both a hardware component as well as a software component, where the hardware component is of heterogeneous nature and may include a combination of ASIC, ASIP, digital signal processors, reconfigurable processors, FPGAs, and general processors. The architecture of digital signal processors has taken many new directions including VLIW, superscalar, SIMD, and more. The choice of the architecture styles and the hardware/software combination are determined by tradeoffs among costs, performance, power, time to market, and flexibility. Furthermore, the boundary between hardware and software has been blurred, while system design is characterized by ever-increasing complexity that has to be implemented within reduced time and resulting in minimum costs. Therefore computer-aided design tools that facilitate easy design process are of essential importance.

The first paper proposes a lightweight floating point arithmetic, a family of customizable floating-point data formats, which bridges the design gap between software and hardware. The effectiveness of the proposed scheme is demonstrated using the inverse discrete cosine transform in the context of video coding. Such flexible data format will find applications beyond multimedia in areas such as wireless communication where a wide range of precision/power/speed/area tradeoffs can be made.

The second paper considers negative cycle detection in a weighted directed graph in the context of high-level synthesis for DSP systems. The paper introduces the concept of adaptive negative cycle detection and demonstrates the application of the technique for problems such as performance analysis and design space exploration in DSP applications.

The third paper introduces a design environment FRIDGE, which supports transformation of signal processing algorithms coded in floating-point to a fixed-point representation. FRIDGE also provides a direct link to DSP implementation by processor specific C-code generation.

The fourth paper presents a technique useful for efficient DSP processor compiler design, which reduces the CPU idle time due to the long memory access latency. The technique explores the instruction level parallelism among instructions of typical DSP applications.

The next three papers deal with ASIC design of various important components such as CORDIC algorithm, FIR filter, and multiplication in GF(2^n). CORDIC algorithm has important applications in Hartley transform, FFT, and DCT. The fifth paper introduces a novel CORDIC algorithm and a novel architecture resulting in the least delay. The sixth paper introduces an efficient parallel FIR filter with a new look-ahead quantization algorithm. Finite field GF(2^n) is of great interests for cryptosystems and the seventh paper introduces a low complexity pipeline multiplier for GF(2^n).

The next three papers discuss efficient implementation on DSP processors for applications in discrete multitone (DMT) communication system, high-speed multimedia communication systems, and image coding. The 512-point IFFT/FFT is a modulation/demodulation kernel in the ADSL systems, and an efficient fast algorithm together with its DSP processor based implementation for IFFT/FFT is derived in the eighth paper. The nineth paper introduces an implementation of point-of-deployment security module on DSP processor (TMS320C6211). The tenth paper develops wavelet engines implemented in DSP platform.

Finally, our last paper presents a full rapid prototyping process by means of existing academic, commercial CAD tools and platforms targeting an architecture that combines multi-DSP with an FPGA.

Overall, we have covered several areas in this special issue: computer-aided design environment, framework, and tools to facilitate the design of complex communication and DSP systems, ASIC based implementation of important components in communication and DSP systems, DSP processor based implementation, and integration of current tools. We thank the authors, reviewers, the publisher, the editorial committee, and the EIC, for the tremendous amount of effort they put into this special issue to make it a success. We believe the readers will find the results presented in this special issue useful for their own design and implementation problems.

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Yuke Wang received his B.S. degree from the University of Science and Technology of China, Hefei, China, in 1989, the M.S. and the Ph.D. degrees from the University of Saskatchewan, Canada, in 1992 and 1996, respectively. He has held faculty positions at Concordia University, Canada, and Florida Atlantic University, Florida, USA. Currently he is an Assistant Professor at the Computer Science Department, University of Texas at Dallas. He has also held visiting assistant professor positions at the University of Minnesota, the University of Maryland, and the University of California at Berkeley. Dr. Wang is currently an Editor of IEEE Transactions on Circuits and Systems, Part II, an Editor of IEEE Transactions on VLSI Systems, an Editor of EURASIP Journal on Applied Signal Processing, and a few other journals. Dr. Wang's research interests include VLSI design of circuits and systems for DSP and communication, computer aided design, and computer architectures. During 1996–2001, he has published about 60 papers among which about 20 papers are in IEEE/ACM Transactions.

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